Design of a Smart Power Manager for Digital Communication Systems

Qusay F. H. Al-Doori

School of Computing, Science and Engineering
University of Salford,
Salford, UK

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Abbreviations.

3GPP	3rd Generation Partnership Project
ALM	Adaptive Logic Module
ASIC	Application Specific Integrated Circuit
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary Metal Oxide Silicon
CRC	Cyclic Redundancy Check
DRP	Digital Radio frequency Processor
DVFS	Dynamic Voltage / Frequency Scheduling
eNodeB	Base Station
FET	Field Effect Transistor
FLC	Fuzzy Logic Controllers
GPP	General Purpose Processor
GSM	Global System for Mobile communication
IEM	Intelligent Energy Manager
IIP	Input Intercept Point
LFSR	Linear Feedback Shift Register
LTE	Long Term Evolution
LTE-A	LTE- Advanced
LTI	Linear Time Invariant
MAPro	Mobile Application Processor
NNC	Neural Network Controllers

PRFP	Pipelined radio Frequency Processor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phased Shift Keying
RF	Radio Frequency
RFFE	Radio Frequency Front End
SDR	Software Defined Radio
SNR	Signal to Noise ratio
SoC	System on Chip
SODA	Signal-processing On-Demand Architecture
SPM	Smart Power Manger

بسم الله الرحمن الرحيم

إِنَّ اللَّهَ عِندَهُ عِلْمُ السَّاعَةِ وَيُنَزِّلُ الْغَيْثَ وَيَعْلَمُ مَا فِي الْأَرْحَامِ ۖ وَمَا تَدْرِي نَفْسٌ مَّاذَا تَكْسِبُ غَدًا ۖ وَمَا تَدْرِي نَفْسٌ بِأَيِّ أَرْضٍ تَمُوتُ ۚ إِنَّ اللَّهَ عَلِيمٌ خَبِيرٌ

(سورة لقمان 34)

Inna Allaha AAindahu AAilmu assaAAatiwayunazzilu alghaytha wayaAAlamu ma fee al-arhamiwama tadree nafsun matha taksibu ghadan wamatadree nafsun bi-ayyi ardin tamootu inna AllahaAAaleemun khabeer

Indeed, Allah [alone] has knowledge of the Hour and sends down the rain and knows what is in the wombs. And no soul perceives what it will earn tomorrow, and no soul perceives in what land it will die. Indeed, Allah is Knowing and Acquainted.

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Dedication.

To my Mother, Wife, and children Omar and Shams

Abstract

Portable devices, like mobile phones, are in an increasing need for power due to the growing complexity of applications and services provided by them. At the same time, mobile devices need to adapt their communication techniques so as to be able to work with different communication standards. The need for a multistandard communication circuit arises to overcome such a problem. Unfortunately, these circuits need to consume a considerable amount of power to achieve their designed goal.

The researchers use the Dynamic Voltage / Frequency Scheduling technique to reduce power consumption in digital systems. This method employs the task time to schedule the system supply voltage along the task time to reduce the overall consumed power. Since the task time in digital communication systems is not defined, the application of the dynamic voltage/frequency technique on such systems is not possible.

In this research, a closer look at the digital circuit power dissipation is given. Then, a new power model is introduced which can predict the digital circuit instantaneous power dissipation accurately. This model is used to build a power control strategy that makes use of the frequency as a control parameter. A setup is carried out using MATLAB to simulate the power of a NOT gate, a multiplexer circuit, a full adder and a two-bit full adder. The results are compared with OrCAD Cadence simulation for the same circuits. The results show that the new model can simulate the power dissipation accurately under different voltages, frequencies, and different technology sizes.

In the second part of this research, a smart power manager is designed based on a fuzzy logic controller. The smart power manager makes use of the measured power and the input frequency to produce the required voltage to the digital system. The smart power manager is tested on a multiplexer circuit, two-bit full adder circuit, and cyclic redundancy check circuits. The results of the simulations show that the manager can reduce up to 60% of the consumed power by these circuits in low frequencies and up to 5% of the consumed power in high frequencies. The smart power manager can fulfil the purpose of the dynamic voltage/frequency scheduling technique without the need for the task time.

In the final part of this research, the Long Term Evolution (LTE) system is taken as a case study. A unique cyclic redundancy check circuit is designed. This circuit is directed to work with LTE systems, so it has three generators integrated into it. The circuit can select the needed cyclic redundancy generator and produce the required remainder for the LTE system. The smart power manager is modified to supply both the voltage and frequency to the new

cyclic redundancy check circuit so that it can control its consumed power. The selection of frequency depends on the used cyclic redundancy generator and the used modulation technique. The selected frequency ensures that the data rate between the LTE stages is constant. The results of the setup show that the smart power manager is capable of reducing the power of the circuit by more than 40% if it was operating at a constant frequency. The smart power manager can lower the power of the cyclic redundancy check circuit by more than 20% if the circuit is running under variable clock frequency.

The conclusion driven from the results above proves that the SPM can reduce the consumed power in multi standard systems and Software Defined Radio (SDR) circuits.

CHAPTER ONE
INTRODUCTION

1.1. INTRODUCTION.

In a digital world, many devices use batteries as their primary source of power. In fact, some of the important factors in the specification of mobile devices are the standby and call times. This figure reflects the ability of the device to consume less battery power and hence its ability to stay on without recharging.

To achieve power reduction in digital systems, designers used many techniques like reducing the technology size, reducing the supply voltage, and even manipulating the application time (Allani, 2011). Many of these methods are efficient, but the problem arises when dealing with communication systems. In such systems, the process time is unknown, the voltage should be fixed, and reducing the technology size has its limits (Rouphael, 2009).

This thesis studies power consumption in digital communication systems with the aim of building a Smart Power Manger (SPM) that can reduce power consumption. Moreover, in this chapter the research problem is introduced then the motivation, the aim and objective of the research. The methodology used to solve the research problem is given followed by the contribution to the science field. Finally, the thesis structure is presented.

1.2. POWER CONSUMPTION IN DIGITAL COMMUNICATION SYSTEMS.

Modern communication circuits consist of two parts, the analogue and the digital circuits (Grayver, 2013; Guizani, 2004). Both of them consume power to produce the required output. Reducing power in both circuits should not affect the functionality of the circuit itself or the integrity of the data processed by the circuit. Unfortunately, reducing the analogue circuit power will reduce the system Signal to Noise Ratio (SNR), and the sensitivity of the receiver which in turn will decrease the system dynamic range (Fernandes & Oliveira, 2015; Rouphael, 2009). On the other hand, reducing power in the digital circuit will not affect the parameters mentioned earlier. Therefore, this thesis is directed toward reducing the power in the digital communication circuits.

To understand how power could be reduced in digital communication systems, a look at the power of the digital systems is needed. This subject is discussed in the next section, and an explanation about how to reduce power in digital systems is introduced. After that, the need for a multi-standard digital communication system is presented so that it is possible to implement the methodology of the research on it.

1.2.1. Power in Digital Systems.

Digital circuits are constructed from logic gates, which in turn are built from Field Effect Transistors (FET). The widely used method in building logic gates is the Complementary Metal Oxide Silicon (CMOS) FET. Hence, a study of how power is dissipated in CMOS circuits will lead to an understanding of how to reduce power consumption in digital circuits. Power in CMOS circuits is consumed in three ways: static, dynamic and short circuit power. These three types of power dissipation may be expressed as (A. P. Chandrakasan, Sheng, & Brodersen, 1992; a P. Chandrakasan & Brodersen, 1995; Pindoo, Singh, Singh, Chaudhary, & Kumar, 2015):

$$P = \alpha . C_L . V_{dd}^2 . F + V_{dd} . I_{Leak} + V_{dd} . I_{sc} \quad (1.1)$$

where P is the power, α is the activity factor (or the probability that the gate will change output from 0 to 1 corresponding to the current input (A. P. Chandrakasan et al., 1992)), C_L is the load capacitor of the circuit, V_{dd} is the source voltage, F is the clock frequency that governs the circuit, I_{Leak} is the leakage current of the FET in ideal state and I_{sc} is the short circuit current of the FET.

From Equation (1.1) it could be noticed that the first term is the dynamic power dissipation, the second term is the static power dissipation and the final term is the short circuit power dissipation. Another thing that is very obvious from equation (1.1) is that power can be reduced significantly by reducing V_{dd}. The method of reducing power through the use of V_{dd} is called Dynamic Voltage / Frequency Scheduling (DVFS) (Ishihara & Yasuura, 1998; Mishra & Tripathi, 2014; Williams & Constandinou, 2013). This method reschedules the voltage along the task time so that, instead of completing the required task as fast as possible with high power consumption, the system will implement the necessary task in the exactly needed time with less power. The best way to demonstrate the efficiency of DVFS is an example.

Consider an individual processor that supports multi-voltage biasing. Given a certain task that needs 10^9 cycles to be executed in its worst case. The maximum time of execution is 25 s. Taking into account that the voltage, frequency and energy consumption are as illustrated in Table (1.1), one can think about the following three task scheduling scenarios (Ishihara & Yasuura, 1998):

Table 1.1: Voltage, Frequency and power consumption for the given microprocessor

Variable	Scenario 1	Scenario 2	Scenario 3
Voltage (V)	5	5, 2.5	4
Frequency (MHz)	50	50, 25	40
Energy Consumption (J)	40	32.5	25

First Scenario:

The processor should work at its maximum performance, leading the microprocessor to operate under 5V supply with 50 MHz clocks and dissipate 40 nJ/cycle. So, the overall time needed for the processor to implement the task is:

1×10^{9} cycles/50MHz=20sec

While the energy consumed during this time is:

$40\times10^{-9}\times1\times10^{9}=40J$

Figure (1.1) illustrates this case by plotting the V^2 against the time where Energy1 is the set that represents this scenario. The plot used V^2 since it is directly proportional with the energy (Jaeger & Blalock, 2008)

Second Scenario:

The processor should work in two schemes to minimise the dissipated power so that the overall execution time could be 25sec. For the first 750 M cycle, the processor will work under 5V V_{dd}, 50 MHz, while for the rest of the 250 M cycles the microprocessor will work under 2.5 V V_{dd} and 25 MHz. Hence, the time needed to complete the task is:

750×10^{6} cycles/50MHz+250×10^{6} cycles/25MHz =25sec.

while the energy consumed during this time is:

$40\times10^{-6}\times750\times10^{6}+10\times10^{-6}\times250\times10^{6}=32.5J$

which is shown in Figure (1.1) by the series Energy2. Moreover, the overall energy improvement is

$$\frac{40J-32.5J}{40J}\times100\%=18.75\%$$

Third Scenario:

The processor should work in optimal voltage of 4 V supply with 40 MHz clocks and dissipates 25 nJ/cycle. Thus, the overall time needed for the processor to implement the task is:

1×10^{9} cycles/40MHz=25sec

while the energy consumed during this time is:

$25\times10^{-9}\times1\times10^{9}=25J$

Again, this is shown in Figure (1.1) in which Energy3 represents this scenario. Moreover, the overall improvement is

$$\frac{40J-25J}{40J}*100\%=37.5\%$$

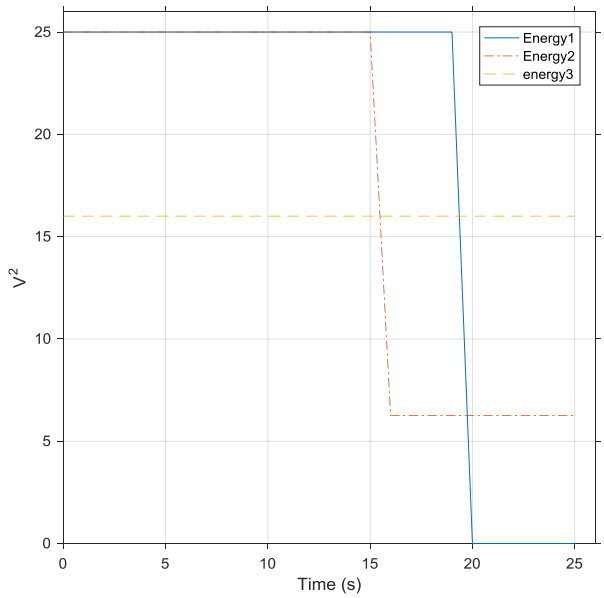


Figure (1.1): Energy Consumption for the Three Scenarios.

The previous example shows that scheduling the voltage can reduce a significant amount of energy in the digital system. Yet, it is worth noting that as the voltage decreases, the frequency decreases too because there is a relation between V_{dd} and the gate delay time as will be discussed in chapter three. Hence, reducing the voltage to reduce the power is not a straightforward method and extra care should be taken not to exceed the limiting parameters of the digital circuit.

Since every digital circuit has its own delay time, it is necessary to know in advance the target circuit to determine the limits of the used supply voltage. For communication systems, many methods are used to transceive signals and hence many digital circuits are used. In the next section, a certain architecture is chosen which is capable of performing most of the communication tasks without the need of changing hardware.

1.2.2. Multi-Standard Communication Systems.

Radio Frequency Front End (RFFE) is the component that will transfer the signal from the radio frequency band to the baseband frequency and make it possible for the receiver to translate the signal into useful data (Grayver, 2013). Due to the massive development in mobile communication, RFFE changed to accept new technology or mobile communication generation. The change in RFFE means that as a new mobile generation evolves, a new RFFE is designed to match it. A problem arises with such evolution: how to design an RFFE that is capable of handling old and new technologies. One solution is to put all the necessary communication circuits in one RFFE to accept all communication generations, but that will consume a lot of power and need bigger space. Another solution is to transfer the signal to digital and hand it to a General Purpose Processor (GPP) to deal with it according to pre-stored algorithms. These algorithms are associated with each communication standard and generation. The last solution is to isolate the communication tasks into a specially designed communication processor that is capable of handling these communication standards (Grayver, 2013).

A question arises: what are the benefits of isolating communication tasks in a coprocessor rather than implementing everything in a GPP or heterogeneous communication ready processor? The answer may lie in the following points:

1- The communication tasks are combined in one chip rather than mixed with another task. Hence, GPP will be free for more non-communication applications (Buss et al., 2003; Krenik, Buss, & Rickert, 2005; Tang, Ambrose, & Parameswaran, 2013b).

2- The separation of tasks will make it easier to analyse and calculate the amount of power wasted due to applying particular communication techniques. Then, it will be simpler to decide which part of the communication algorithm is consuming the largest amount of energy (Tang et al., 2013b; Woh et al., 2006).

3- If the coprocessor software and hardware are adaptable to the used communication algorithms, then this will make it easier to modify them to accept changes in the standards and communication needs, i.e. increase their functionality (Tang, Ambrose, & Parameswaran, 2012; Tang et al., 2013b).

4- If the coprocessor software and hardware are reconfigurable, then it is easier to implement new technology on such a device, leading to an increase in the adaptability of the system (Tang et al., 2012; Tang, Ambrose, & Parameswaran, 2013a; Tang et al., 2013b).

The reason behind discussing coprocessors is to analyse and review the work of (Tang et al., 2012, 2013a, 2013b) who built a pipelined communication coprocessor capable of working in a multi-standard environment with low power consumption. The research objective of minimising the power consumption of the mobile device will be based on their work.

Designing a multistandard communication system is part of the Software Defined Radio (SDR) area. (Mitola, 1993) defined SDR as a group of simple DSP functions that are directed toward communication purposes and gathered into a processor-based system. (Krenik et al., 2005; Krenik & Yang, 2003; Muhammad, Staszewski, & Leipold, 2005) declared that the best way to produce a multi-standard digital transceiver is by using a processor (either GPP or Application Specific Integrated Circuit (ASIC)). This processor will implement different Radio Frequency (RF) tasks for a different standard.

Throughout the literature, it was found that there are four basic architectures to work as multi-standard digital communication transceivers:

1- Digital Radio frequency Processor (DRP™) of (Faust, 2008; Muhammad et al., 2005; R. Bogdan Staszewski, Muhammad, & Eliezer, 2007; R. B. Staszewski, Muhammad, & Leipold, 2006; RB Staszewski, Muhammad, & Leipold, 2005; Roman Staszewski et al., 2006; Roman Staszewski, Jung, Staszewski, Leipold, & Murphy, 2007; Stazewski, Hung, & Fei, 2009). It is a DSP processor dedicated to working for mobile and wireless applications.

2- System on Chip (SoC) for Global System for Mobile (GSM) communication of (Bonnaud et al., 2006), which are specially designed analogue and digital circuits for GSM applications.

3- Signal-processing On-Demand Architecture (SODA) of (Woh et al., 2006) which is a multicore DSP platform capable of implementing SDR.

4- Pipelined radio Frequency Processor (PRFP) (or Mobile Application Processor (MAPro)) of (Tang et al., 2012, 2013a, 2013b) which is a pipelined communication coprocessor for wireless communication.

Table (1.2) shows a quick comparison between these four architectures regarding power consumption of the device, method of functional control, the adaptability of the system, the ability of the system to accept new technology and the overall throughput.

DRP and SoC for GSM are both designed as communication processors without any consideration to power consumption i.e. no power reduction method is listed in the literature, while SODA and the PRFP were designed with power consideration as a design factor but the only method used in the design is the shutdown technique. Another drawback in the SODA design is that its four processing elements take a lot of space and power management. The above discussion makes the PRFP in the lead of this comparison for power consumption.

The unique design of the PRFP with its reconfigurable communication pipeline would make it superior over other processors since the overhead of the GPP is less than the others, or in another word, is easier to control. Another feature that makes this processor in the lead of Table (1.2) is its adaptability to different communication standards through adaptable pipeline stages that can be easily changed. Finally, PRFP and SODA have a higher throughput than that of other architectures since other designs use only one processing unit to calculate the output while SODA uses four DSP processing elements compared to ten pipelined stages in PRFP.

Table 1.2: comparison between different RFP architecture

Architecture	power Consumption	Hardware / Software	Adaptability	Upgradable	Throughput
DRP ™	Not listed	Fully software controlled	limited	Limited	Low
SoC for GSM	Not listed	Fully software controlled	Limited	Limited	Not available
SODA	Medium	Fully software controlled	Limited	Limited	High
PRFP	Low	Software and Hardware controlled	High	High	High

The adaptability, upgradability, throughput, and low power consumption of PRFP made it a perfect choice for this research for its architecture to be used in a new coprocessor that consumes less power and can work with different communication standards.

1.3. RESEARCH PROBLEM AND OBJECTIVES.

Power consumption in mobile devices is the concern of many researchers. Many areas are affected by this subject. The following list gives some of these areas:

1- The analogue communication circuit: Reducing power in this stage can widely affect the mobile network quality of service since it affect the SNR, the dynamic range…etc. (Fernandes & Oliveira, 2015; Rouphael, 2009). These parameters are very important to maintain a good communication link between the mobile device and the base station (eNodeB). If the battery power is reduced then this stage will not function properly.

2- The mobile device screen: (Carroll & Heiser, 2010) showed that there is a considerable amount of power that is consumed in the mobile device screen specially when the backlight is in use. Battery life time can affect the visibility of the screen especially when the battery is at low level of charge.

3- Mobile applications: the services provided by the mobile device these days, bypassed its elementary job which is communication, to other areas. Nowadays you can play video games, watch movies, and book a place in a theatre or football game, even pay for your groceries from your mobile device. These applications consume a considerable amount of power, and for a mobile device the power source is the battery (Murmuria, Medsger, Stavrou, & Voas, 2012).

The above list shows some of the systems that consumes power in mobile devices. All these systems get their power from the mobile device battery which should be large enough to supply all the needed power and in the same time, of a small size and weight to keep the mobile device small (Satyanarayanan & Mahadev, 2010). Usually, mobile device manufacturers uses small batteries to reduce the size and weight of the device which increase the need for recharging these devices (Cope & Podrazhansky, 1999). To reduce the urgency of the need for recharging the device battery, the designers tries to reduce power consumption in the individual systems of the mobile device and that what drives this research.

Section (1.2) showed the efficient ability of the DVFS method in reducing power. Besides, it revealed that PRFP could be used for different communication standards with low power consumption. According to (Tang et al., 2012, 2013b), PRFP power could further be reduced using DVFS. Yet, how much is the task time in communication systems? Would the

reduction of voltage affect the working frequency of the system? Is the integrity of data affected by the voltage change? Many questions need to be answered in this thesis, but the main research question is

"How to reduce the mobile device power?"

There must be a mechanism to make use of the mobile device working parameters to reduce its power. This mechanism should decide when and how to reduce the consumed power. Hence, the research problem is to find a method to reduce power in the digital communication system of the mobile device.

1.4. The Aim and Objectives of the Research

The research is motivated by the need for low power technology in the RFFE capable of accepting new communication standards and technologies without affecting the performance of the device. Its aim is to build an SPM unit that is capable of reducing power in the digital communication system of the mobile device utilizing the frequency changes that may occur due to the changes in the used communication standard.

Realising the research problem should pass through many steps. For this research, the steps are:

1. Analyse power consumption in digital circuits. Understanding how the power is consumed in CMOS circuits and the parameters that affect it, will lead to a better utilisation of this parameter in order to reduce power.
2. Modelling power consumption in digital systems. Building a mathematical model of the power consumption in digital system will provide a test bench for any method of power reduction that needs to be tested. Hence an accurate model for the power in digital systems is needed.
3. Implement the components of a multistandard communication system. The elements of the digital communication system in a mobile device should work with the multistandard communication system. Implementing them will build a test bench for the SPM to prove its ability to reduce power.
4. Make use of the system frequency as a governing parameter to reduce power. The multistandard communication system works with different frequencies set by the communication standard. This diversity of frequencies could be used as governing parameters to the SPM.

5. Design an SPM based on DVFS. In digital systems, DVFS generate a schedule for the voltage to control power based on the task time of the process. Utilising the frequency differences that exist in multistandard communication systems, an SPM can be designed. This unit uses DVFS as the main power reduction algorithm. The DVFS algorithm should be modified to accept frequency changes rather than task time to produce the required voltage for the system.
6. Test the SPM unit to prove its ability to reduce power. A setup is made from some components of the multistandard communication system using the results of steps one and two, to show the ability of the SPM to reduce power in Digital communication systems, The SPM was designed using step five and tested using setup three and four. The power of the system was measured using the power model obtained from step one, and hence the ability of SPM to reduce the power was proven.

1.5. METHODOLOGY

This thesis depends on a mixed methods of analyses, simulations and experments. The general method of reducing power in digital communication circuits is shown in Figure (1.2) which describes the major steps that govern the plan of this research.

The first phase in the methodology is to review the literature that deals with power reduction in digital circuits with a particular focus on the communication system. The review will give a clear understanding of the methods used to reduce power in digital circuits and the best method that can be implemented on digital systems.

The second step will look at the parameters that affect the power equations in the digital circuits to understand its behaviour under different circumstances.

Based on the understanding that was built in step two, step three will propose a solution to reduce power in the digital communication circuits. This solution is to create SPM that makes use of the variation in the value of the parameter due to the use of different standards. The aim of the SPM is to reduce the circuit's consumed power.

In step four, the mathematical model of power consumption is derived. This model should contain all the parameters that affect power in digital communication systems. The model will be used in step six to measure the amount of power reduced when using SPM.

The SPM unit should make use of the parameters that were studied in step two and three. Step five uses these parameters to design the SPM which is capable of reducing the system power according to the used communication standard.

Step six is to simulate the overall system with the SPM unit, and then to make use of the mathematical model that was derived in step four, to calculate the system power.

Depending on the power measurements that was made in step six, step seven will redesign the SPM unit so that the power reduction is at its maximum value.

When the maximum power reduction is reached, analysis and conclusion of the research are done in step eight.

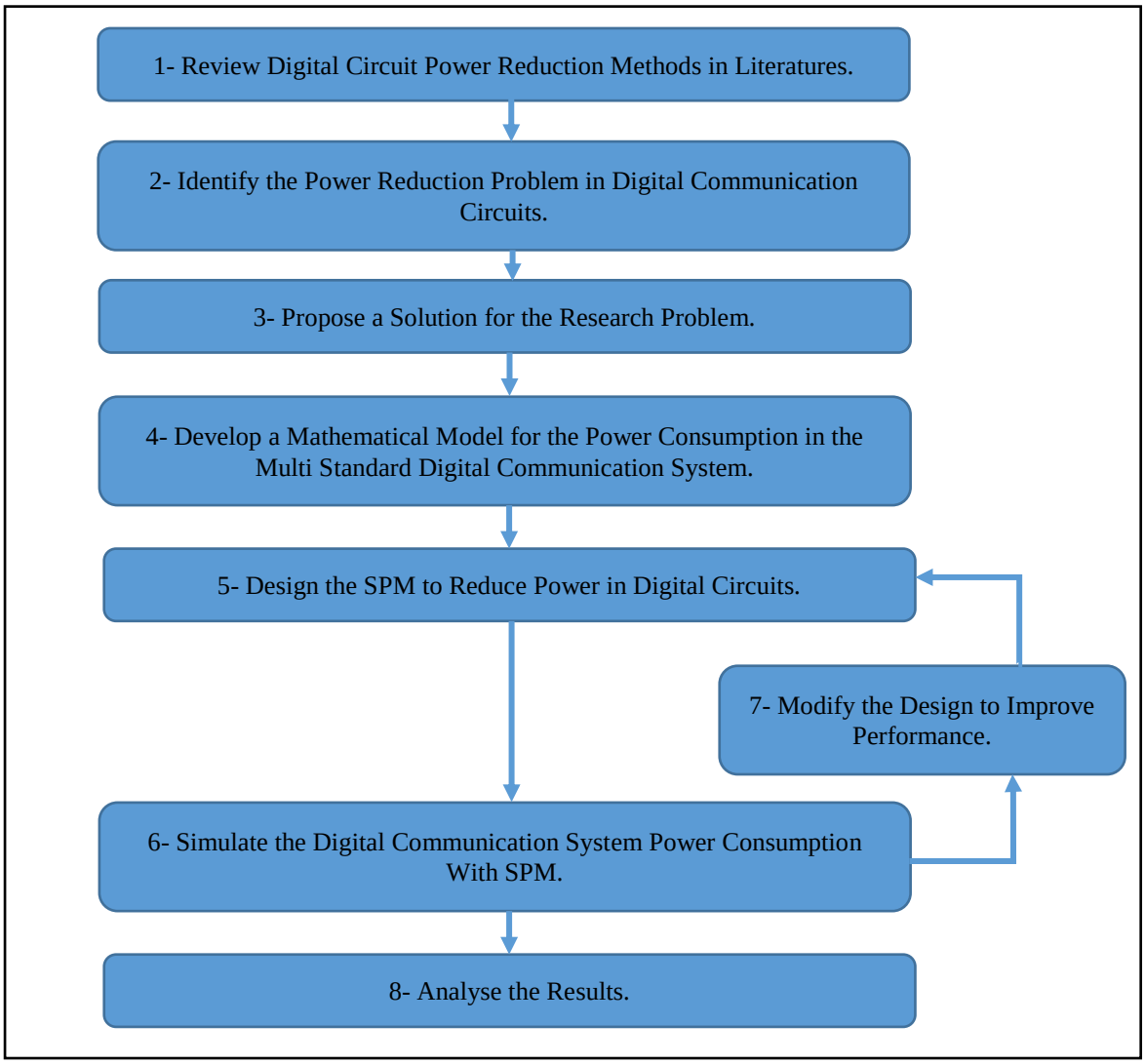


Figure (1.3): Research Methodology.

1.6. CONTRIBUTION TO KNOWLEDGE.

Throughout the research process described in (1.5), the researcher managed to add five contributions to the field of knowledge. Some of these contributions are published in conferences and journals, while the others are listed in this thesis. The major contributions that were made in this research are:

1- Building an algorithm to calculate the dynamic power dissipation in digital circuits. Studying the literature of power management in digital circuits showed that the dynamic power model is very primitive. Hence, a new model was derived by including the following parameters in the model:

- The technology size.
- Digital circuit architecture.
- Inputs randomness.
- Circuit delay time.

The new model dynamic power was compared with simulation results taken from OrCAD Cadence software for some circuits. The results showed that the new model could simulate the dissipation of the dynamic power efficiently.

2- The real relation of frequency and dynamic power was observed. By implementing the new dynamic power model on different digital circuits, the relationship between frequency and power is recognised as nonlinear, while the old model shows that the relationship is linear. Frequency effect on the dynamic power can be influenced by the randomness of the circuit inputs and the architecture of the circuit itself.

3- Using the frequency as a governing parameter to reduce power. After analysing the behaviour of the dynamic power corresponding to the frequency, it was possible to build a control algorithm to the power based on frequency changes that may occur in the digital circuit.

4- Building a Cyclic Redundancy Check (CRC) circuit capable of working with different generators. Through the study of the multistandard communication system, it was possible to produce an algorithm capable of generating a multi-polynomial CRC circuit. The algorithm was used to build a CRC circuit for the Long Term Evolution (LTE) communication system.

5- Building the SPM to reduce the digital communication circuit dynamic power. By making use of the frequency changes, and the new power model that is described in chapter three, an SPM was designed to reduce power in the digital communication circuits. The SPM was tested on different systems to prove its ability to reduce power. Finally, a case study was made to implement the SPM on the LTE system. The implementation proved that SPM could reduce no less than 40% of the consumed dynamic power in such systems.

1.7. THESIS ORGANISATION.

This thesis is divided into eight chapters. The first one introduces the power consumption problem in a multistandard communication system, the methodology to solve it, and the contribution to knowledge that is gained from this research.

The methods of power reduction in digital circuits are presented in chapter two. The chapter will also introduce a critique to these methods from communication circuits point of view. After that, a method is chosen to be implemented on the digital communication circuits.

Chapter three will presents the mathematical model for the dynamic power consumption in the digital gates. A discussion about how power is consumed in a digital circuit is to be introduced to build a more robust mathematical model for the dynamic power. The new model includes the technology size, and the circuit architecture to produce a precise measure of the consumed dynamic power of the circuit. Finally, to prove the accuracy of the new model, a comparison between the power calculated using the new model and the power measured using OrCAD Cadence software is made using some digital circuits.

The design of the SPM unit is made in chapter four. The design is based on fuzzy logic reasoning, and it will take advantage of the system frequency to produce the best supply voltage to the system. The design is based on DVFS technique but with the substitution of the task time by the frequency. The SPM was tested with 2×1 MUX and two-bit full adder circuits to prove the ability of SPM to reduce the dynamic power.

Chapter five discuss how to design parallel CRC circuits especially the 8, 16 and the 24 bit CRC that are used in the LTE system. The chapter will further introduce a single CRC circuit that is capable of producing the required remainder of the 8-bit, 16-bit and the 24-bit generator in one circuit, i.e. with a lower number of gates and hence less power consumption.

The SPM is connected to the CRC circuits in chapter six to prove its ability to reduce power in digital communication systems. The test was carried out on different CRC circuits to demonstrate the ability of the SPM to work with various circuits.

In chapter seven, a case study is made in which the SPM is modified to supply not only the voltage of the system but also produce the required clock frequency of the LTE CRC system. The frequencies are generated according to the required modulation technique and the used CRC generator. The power of the system is measured to show the ability of the SPM to reduce power in the LTE systems.

The eight and the final chapter is the conclusion and discussion. In this chapter, the thesis is concluded, and the results are discussed. At the end of this chapter, future work is suggested.

CHAPTER TWO

POWER REDUCTION IN DIGITAL SYSTEMS

2.1. INTRODUCTION.

Notebooks, laptops, mobile phones, tablets, etc., are all examples of digital systems that use batteries as the main source of power. Since the operation of these devices consumes a lot of power, the battery will not be able to supply energy to these devices for a long time without recharging. A question to ask here is how to reduce power in such devices? The answer lies between the factors that affect power consumption in the digital circuits. Another question arises which is how digital circuits consume power? Are all types of power consumed in a digital system useful? This chapter tries to answer these questions and to find a mathematical relationship between power consumption and the factors that affect it.

This chapter is divided into four sections in which the types of power dissipation are listed and the power reduction methods in digital systems are discussed. Then, the parameters that effect dynamic power consumption are introduced. Finally, a discussion is presented about what other parameters affect dynamic power consumption, which are not taken into consideration in the current power models.

2.2. POWER DISSIPATION IN CMOS CIRCUITS.

There are three types of power dissipation in CMOS circuits, as mentioned in section (1.2.1). These types are static, dynamic, and short circuit power dissipations. Equation (1.1) gave the expression for each type of these power dissipations. Since there are different power dissipation types and each depends on different variables, then there will be many methods that facilitate these variables to reduce the corresponding power dissipation type (Allani, 2011). In this section, the types are briefly described to determine the factors that can be used to reduce the overall power dissipation in logic circuits.

2.2.1. Static Power Dissipation

When the logic gates input is not changing, the only power dissipated in the circuit is the power needed to keep the value of the gates on the high or low states. This power is called the static power. In the early investigation of power dissipation in logic gates, this power was considered zero since its effect is negligible with respect to the more dominant dynamic power dissipation (Martin, Flautner, Mudge, & Blaauw, 2002). As the IC scaling technology evolved, static power dissipation started to appear because the effect of dynamic power in VLSI was no longer the dominant power dissipation type (Martin et al., 2002).

In a general logic circuit and according to equation (1.1) the static power dissipation (P_s) is given by:

$$P_s = V_{dd}.I_{Leak} \quad (2.1)$$

In FET, static power dissipation is giving by:

$$P_S = V_{DD}.I_{subn} + |V_{bs}|.\left(I_{jn} + I_{bn}\right) \quad (2.2)$$

I_{subn} is the sub threshold leakage current, I_{jn}, and I_{bn} are the drain and source to body junction leakage currents in the N channel MOS (NMOS) devices and V_{bs} is the base to source voltage.

I_{subn} is given by:

$$I_{subn} = \left({}^{W}/_{L}\right).I_s.\left[1 - e^{\frac{V_{DD}}{V_T}}\right].e^{\frac{-\left(V_{th}+V_{off}\right)}{n.V_T}} \quad (2.3)$$

W, L are the FET width and length respectively. I_s, n, and V_{off} are empirically determined constants for a given process. V_T is the thermal voltage and V_{th} is the threshold voltage of a short channel MOSFET in Berkeley Short-channel IGFET Model (BSIM) model (Z. Liu et al., 1993; Martin et al., 2002).

As shown in (Martin et al., 2002) the relation between V_{th} and V_{bs} is linear and it is given by:

$$V_{th} = V_{th1} - K_1.V_{DD} - K_2.V_{bs} \quad (2.4)$$

where V_{th1}, K_1 and K_2 are constants.

Substituting equation (2.4) into (2.3) and making use of the fact that V_{off} is typically small and the term $(1 - e^{\frac{V_{DD}}{V_T}})$ is approximately 1, then equation (2.3) becomes:

$$I_{subn} = K_3.e^{K_4.V_{DD}}.e^{K_5.V_{bs}} \quad (2.5)$$

K_3, K_4 and K_5 are constants.

Equation (2.5) implies that a reduction in V_{bs} will reduce the power of the logic circuit because it reduces the leakage current. Yet, since V_{bs} is governed by the technology size, i.e. as the channel width decreases, V_{bs} will increase, so there is a restriction to this method. To sum up, although there is a restriction to the used value of V_{bs}, reducing it will reduce the total amount of consumed static power. This reduction is considered when the technology size is less than 90nm because after this size, static power dissipation may take 30% of the overall power dissipation of the logic circuit (Jaeger & Blalock, 2008; C. Kim & Roy, 2002)

2.2.2. Short Circuit Power.

When a CMOS circuit switches its state, there will be a short time when both the PMOS and the NMOS transistors are in the ON state. This short period of time will allow the

short circuit current to flow from the supply to the ground (Allani, 2011). This current depends on V_{dd} and the threshold voltage V_{th}. the power associated with this current is given by (Allani, 2011; Jaeger & Blalock, 2008; Paul, Agarwal, & Roy, 2006):

$$P_{sc} = \frac{\beta}{12}.(V_{dd} - V_{th})^3.\tau.f \quad (2.6)$$

Where β is the transistor voltage gain, τ is the time duration that both the NMOS and the PMOS transistors are in the ON state, and f is the frequency.

Short circuit power could be reduced by reducing V_{dd}, V_{th} and f which are the same parameters that affect the dynamic power dissipation.

2.2.3. Dynamic Power Dissipation.

Each time a logic gate changes state from 0 to 1 or 1 to 0, current flows from the power supply to charge load the capacitor of the gate leading to power being consumed. The power associated with this state change is given by (Allani, 2011; Ishihara & Yasuura, 1998; Jaeger & Blalock, 2008; Nielsen, Niessen, Sparso, & van Berkel, 1994):

$$P_d = \alpha.C_L.V_{dd}^2.f \quad (2.7)$$

Where P_d is the dynamic power dissipated in the logic circuit or the power dissipated due to the gate state change.

Many research papers dealt with this type of power and used the parameters of equations (2.7) in different ways to reduce the consumed power (Bonnoit, 2010; Flynn & Rives, 2003; Ishihara & Yasuura, 1998; Zang & Gordon-Ross, 2013) because this type of power dissipation dominates over digital power consumption (Jaeger & Blalock, 2008).

The dynamic power dissipation will be discussed in more details in chapter three to emphasise on its parameters and how it can be used to reduce the digital circuit power.

2.2.4. Glitch Power.

To understand the concept of glitches, consider the logic circuit shown in Figure (2.1) in which the NOT output appears after its input changes in 10 nsec. The AND gate will produce the output after 8 nsce. Please note that the numbers in this example are for illustration only and do not represent the actual values of the gate delays. Initially, assume that the A input is at a low state (logic 0) and that it will change state to logic 1 after 5 nsec. Figure (2.2) is the timing diagram of the circuit and it shows the change in the value of A at 5 nsec. Although A is

changing from 0 to 1 at 5 nsec, B will have to wait for another 10 nsec (i.e. until 15 nsec passes) to produce the output due to the NOT gate existing delay. This delay will deceive the AND gate and put its input into the (11) condition that must produce an output of 1. Such output of the AND gate should appear after 13 nsec (5 nsec for the input change and another 8 nsec for the output delay), but after 15 nsec, B is corrected and changes its state to logic (0) which will affect the output of the AND gate (Op) to go back to logic (0) again. This change in the output will take an additional 8 nsec to appear in the circuit output (Op).

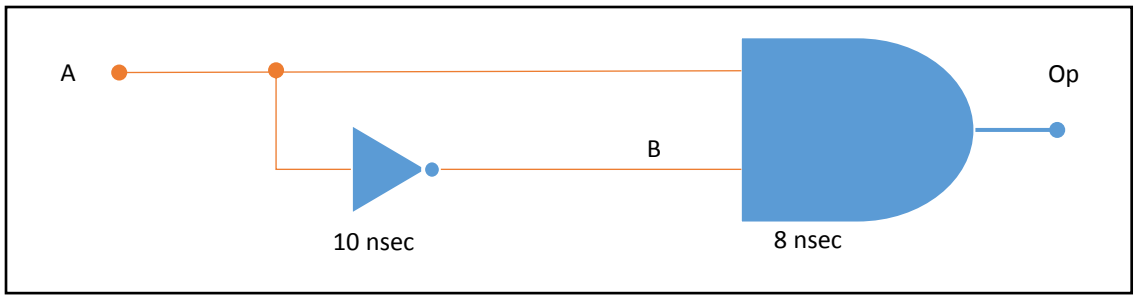


Figure 2.1: Example of a Glitches Logic Circuit.

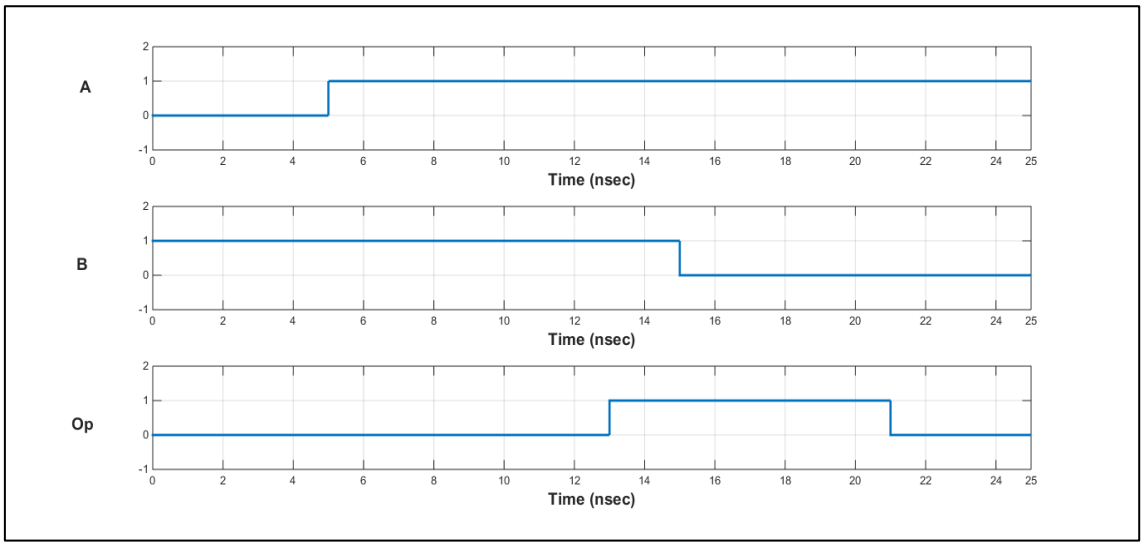


Figure 2.2: Timing Diagram of the Circuit Output Glitches.

Although it is expected that Op stays at logic 0 at all time, the delay effect causes Op to change state to logic (1) at 13 nsec then back to logic (0) at 21 nsec. This error in the output is called a glitch and it consumes some part of the total dynamic power of the circuit. Modelling of this kind of error depends on the behaviour of the circuit input, delay times of the gates in the digital circuit, and the technology size of the digital circuit (Favalli & Benini, n.d.; Omana, Papasso, Rossi, & Metra, n.d.).

Glitches produce an unwanted behaviour in the circuit output, so the power that these glitches consumes are wasted and should be minimized. One way to do so is by manipulating the time delay of the circuit so that the inputs of a certain gate are all delayed by the same factor (Chou & Hung, 2015; Huda & Anderson, 2016; Majumder, Kaushik, & Mondal, 2016).

2.2.5. Digital Circuits Power Consumption Effecting Parameters.

From the discussion made in the previous sections, it can be shown that the main parameters that affect power consumption in a digital circuit are:-

1- The supply voltage (V_{dd}).
2- The threshold voltage (V_{th}).
3- FET size (W/L).
4- Biasing voltage (V_{bs}).
5- Load capacitor (C_L).
6- Activity factor (α).
7- Frequency (F).

It should be noted that although the glitch power was discussed separately, it is still part of the dynamic power consumed by the digital circuit. Therefore, any method that reduces the dynamic power consumption will by default reduce the glitch power.

The applied power reduction methods use one or more of the mentioned parameters to establish the needed reduction. Some of these methods reduce only one type of power consumption, others reduce more than that. The method capable of reducing V_{dd} can reduce all the power consumed in the digital circuit.

2.3. POWER DISSIPATION REDUCTION METHODS

In the previous sections, the types of power consumption in digital circuits were discussed and the parameters that can affect these consumptions were clarified. In this section the methods used to reduce the consumed power are introduced briefly. This illistration will be used later to build a comparison between these methods so that the best method is chosen as a base for this research.

2.3.1. Power Gating (Shutdown) Method.

Power gating is widely used in microprocessors and memory circuits. It reduces the static power by cutting off the supplied voltage to the unneeded cores or part of the circuit.

(Jaeger & Blalock, 2008; Piguet, 2006). Figure (2.3) shows the power gating circuit, where T1 and T2 are two PMOS transistors used to cut the power supply of Logic block A or B if the block is not needed. This method will efficiently reduce static power. Yet, a problem arises when a block is needed after shutdown. It needs time to recover to a functional state, which will reduce the efficiency of the method (H. Kim, Shin, Hyung-Ock Kim, & Youngsoo Shin, 2006; Paul et al., 2006; Shi & Howard, n.d.).

It should be noted that this method reduces only the static power in part of the digital circuit. It is used in a multi core processor environments or memory bank when the stored data are small with respect to the memory size. Its use in digital communication systems is limmited to the pipelined architectures such as PRFP since it can shutdown some of its stages according to the used communication standard (Tang et al., 2012, 2013a, 2013b)

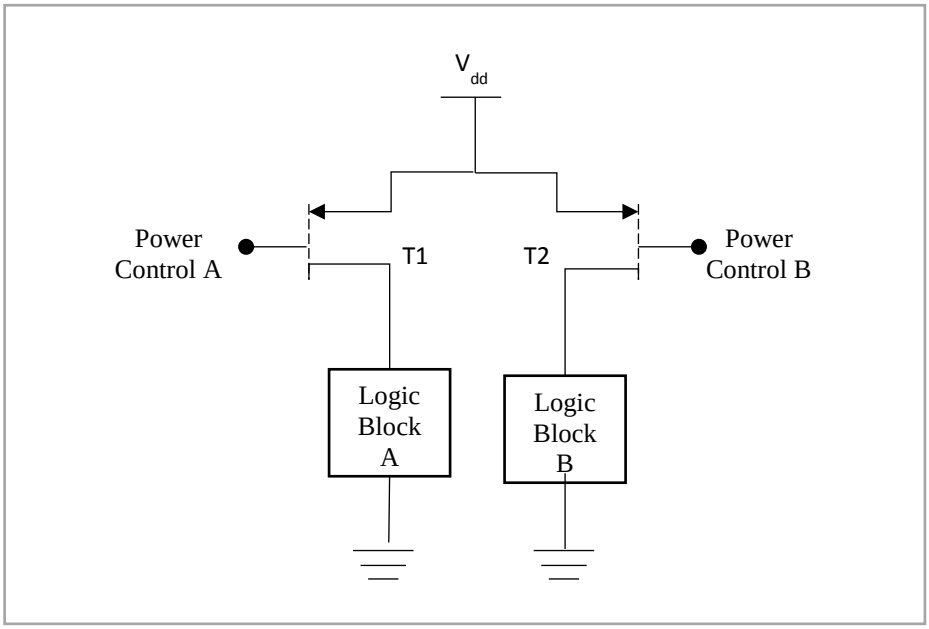


Figure 2.3: Reducing Static Power with Shutdown Technique.

2.3.2. Clock Gating (Sleep Mode) Method.

In the clock gating method, the clock is gated using AND gate so that the circuit that is fed by the clock is governed by a control signal. This control signal will switch the clock on or off to the circuit putting it in either idle (sleep) state or active state (Gluzer & Wimer, 2017; Mahmoodi, Tirumalashetty, Cooke, & Roy, 2009; Qing Wu, Pedram, & Xunwei Wu, 2000; Tschanz et al., 2003). The circuit used to gate the clock is shown in Figure (2.4).

It is worth noting that this method will only reduce the dynamic power consumption. It will put the circuit into sleep mode so that whenever the circuit is needed, the clock lock is open and the circuit is back into active mode without any delay. This method could be used in digital communication processors and systems since it does not eliminate the function of the stages it controls. Instead, it just puts it into sleep until the stage is needed. Nevertheless, this method can only reduce the dynamic power dissipation since the clock controlled stage will consume static power even in its sleep mode.

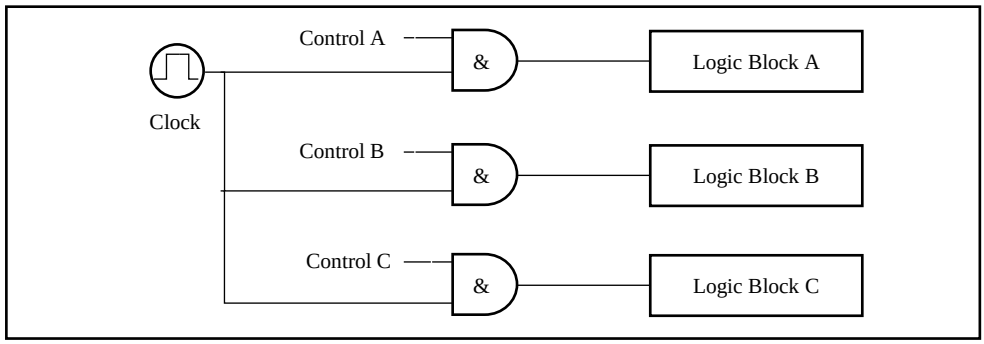


Figure (2.4): Clock Gating Power Reduction Method.

2.3.3. Technology Scaling Method

As it was shown in equation (2.3), if W/L value is reduced, the static power will be reduced. Hence, a reduction in the technology size can decrease the consumed power. This is true not only for the static power but also for the dynamic and short circuit power consumptions (De & Borkar, n.d.; Horowitz et al., n.d.; Keshavarzi et al., 1999; Srinivasan, Adve, Bose, & Rivers, 2004). This effect comes from the fact that technology scaling can reduce the supply voltage V_{dd}, and the threshold voltage V_{th} of the logic circuit (Y. (Kevin) Cao, 2006; EnOcean, 2011). The effect of technology size on power will be demonstrated later in section (3.5) where a simulation of some circuits shows clearly this relation. Unfortunately this reduction in the size is limited' by Moore law (Schaller, 1997; Z. Yu et al., 2017) where sizing can only be minimized to certain limits after which the generated heat in the FET will forbid the industry from building smaller transistors.

2.3.4. Big Little Architecture.

This method may be the newest among power reduction techniques in digital systems. In fact it works with multi core processors and was designed specifically for mobile devices (Castro et al., 2015; M. Kim, Kim, Geraci, & Hong, 2014; K. Yu, Han, Youn, Hwang, & Lee, 2013; Yuhao Zhu & Reddi, 2013). The method separates the tasks according to the needed

performance and uses a specially designed microprocessor that contains at least two cores. The first is a high performance core that consumes a large amount of power, while the second core is of a low performance and consumes less power than the first core. If the task requires powerful calculation and the results are needed very fast, the data flow is directed to the high performance core. If the task does not need performance then the data are directed to the low performance core to reduce power (Greenhalgh, 2011; Jeff, 2012). This method can efficiently reduce power in mobile devices but it looks to the digital circuit from a higher perspective, which makes it suitable for power reduction in digital systems rather than digital circuits. Another point that should be mentioned against this method is that communication tasks are all directed into the DSP cores in multi core communication processors. This last point limits the use of this method in digital communication circuits.

2.3.5. Dynamic Voltage Frequency Scheduling (DVFS) Technique.

The basic functionality of DVFS was discussed in section (1.2). Actually, this method is called Dynamic Voltage Scheduling in most of the literature. The addition of the word "Frequency" came from the fact that changing the voltage will change the circuit output propagation time, and, thus, affect the maximum operation frequency of the circuit. This relation will be introduced later in section (3.2).

DVFS is not a new method. It arises from research on power reduction in digital audio and video recording devices (Z. Cao, Foo, He, & Van Der Schaar, 2010; A. P. Chandrakasan et al., 2010; Kurdahi, Eltawil, Yi, Cheng, & Khajeh, 2010; Nielsen et al., 1994). The first time DVFS was introduced to microprocessors was in (Ishihara & Yasuura, 1998) where the method was discussed and theories for the best voltage set per task is laid. (Zhai, Blaauw, Sylvester, & Flautner, 2004) showed that it is possible to reduce V_{dd} even to lower than $V_{dd}/2$ or to a sub threshold level which leads to power reduction of more than 25% of the dynamic power. More advanced research on the effect of using different loads (switches) to implement the same task is made by (Kwon & Kim, 2005) in which DVFS technique is modified to choose not only the best voltage scheduling but also the best core to execute the task. The effect of soft error susceptibility while implementing DVFS is addressed in (Chandra & Aitken, 2008) alongside the effect of minimizing the technology to the 45 nm scale. The impact of voltage transition on the cores of the processor are discussed in (W. Kim, Gupta, Wei, & Brooks, 2008) and the proposed switching regulators are introduced to each core to enhance power reduction.

Another improvement to the method is the ability to work in multiprocessor platforms which maintain the performance for executing the user program. Further investigation on the role of the operating system on ARM 11 platforms is given in (Tsao & Chen, 2012) which addressed the power management problem in embedded systems and the ability of the operating system to solve this problem. The method is further enhanced in (Ozturk, Kandemir, & Chen, 2013) where the scheduling was made in the compiler stage by taking information not only from the task history and time but also from the power islands and the shutdown routines in these islands.

The above-mentioned researchers controlled the voltage scheduling through the operating system. It is not efficient in the case of communication systems since the task time is unknown, which eliminate the voltage scheduling operation.

An introduction to a special hardware that will perform DVFS on the processor according to the processor's workload is given in (Flynn & Rives, 2003). The dynamic workload of the processor is measured by an Intelligent Energy Management (IEM) unit to determine the needed change in the supply voltage so that power consumption is at its lowest rate. Another enhancement is made by (Hamid Reza Pourshaghaghi & de Gyvez, 2009) in which the core current is measured and used to supply feedback to a Fuzzy Logic Controller (FLC) that will decide the new set of voltage to be applied to the core. FLC was yet to be used by (Tapou & Al-raweshidy, 2012; Tapou, Al-Raweshidy, Abbod, & Al-Kindi, 2011) to control a buck convertor circuit that will supply the voltage to the processor featuring different loads. The methods mentioned in this paragraph changed the voltage of the processor according to the current or load of the processor regardless of the task time of the process. This development makes this method applicable to communication systems.

2.4. Power Reduction Method for Digital Communication Systems.

In the previous section, the methods that are widely used to reduce power in digital systems were discussed. In this section, it is required to choose a method that can be applied into the multi standard communication system so as to efficiently reduce the consumed power. A comparison was made between the power reductions methods listed earlier to choose the right method that could be applied to the multi standard communication system.

The results of the comparison is given in table (2.1). Note that the technology scaling is eliminated from the table because the required method should work with the multi standard

communication system regardless of the technology size. Since DVFS reduces V_{dd}, it can reduce the overall power consumption because V_{dd} contributes to all power consumption types. This fact is shown in the first row of table (2.1)

The difference between a digital system and a digital circuit is that the digital system consists of one or more than one digital circuit. Since big little techniques work with only multi core processors then it cannot be implemented on digital circuits.

The parameters that influence the efficiency of the methods are shown in the fifth row of table (2.1) where the wakeup time is a critical issue for the power gating technique, while applying big little technique on small circuits is not possible. DVFS suffers from the fact that when it reduces the voltage, the maximum working frequency is reduced as well, which limits its ability to reduce power in very high frequency systems.

Table 2.1: A Comparison between the Power Reduction Methods

Parameters	Power Gating	Clock Gating	Big Little Architecture	DVFS
Targeted Power Consumption	Static	Dynamic	Dynamic	All
Applicability to Digital Circuits	Yes	Yes	No	Yes
Applicability to Digital Systems	Yes	Yes	Yes	Yes
Applicability to Communication Systems	Yes	Yes	Yes	Yes
Limiting Parameters	Wake up time after shutdown	N/A	Works only on multi core systems	Limited by the minimum and maximum values of V_{dd} and F
Controlling Entity	Software	Software	Software	Hardware / Software
Power Reduction Efficiency	Mid	low	Mid	High

DVFS could be controlled by either software in which it can reduce power for a digital system, or it can be controlled by hardware such as IEM (Flynn & Rives, 2003) to reduce power in digital circuits or systems.

Finally, the efficiency of power gating is mid since it can eliminate power consumption from part of the system for a certain period of time. When the module that has been shut down is needed, it will consume power again. The same thing applies to clock gating. Big little architecture reduces power efficiently but it can be improved if the processor voltage is reduced.

DVFS was used with all the mentioned techniques since it can reduce power efficiently. Most of the microprocessors now a days use this technique as the norm of the power stage in the processor.

Due to the previous discussion, DVFS was considered in this research as the main method that the SPM unit will use.

2.5. Summary and Conclusions

In this chapter, the types of power consumption in digital systems were discussed. Three equations were illustrated to find the parameters that are used to control power consumption in digital systems. After that, the methods of power reduction in digital circuits and systems were introduced and compared to find the best method to be used in the multi standard communication system. DVFS was chosen to be the best method available for this purpose.

It was noticed that the effect of the number of bits that a system uses on power was never discussed in the literature. Another important factor is the used technology size and its impact on the consumed power. These factors will be discussed in the next chapter so that they are all included in a mathematical model that describe power consumption in digital systems.

CHAPTER THREE

DIGITAL CIRCUITS POWER MODEL

3.1. INTRODUCTION.

A key aspect of the digital circuit design is the power consumed by the circuit. It determines the overall power consumption of the device, and hence, the needed power supply model and battery capacity (Ishihara & Yasuura, 1998; Pindoo et al., 2015). Another important need for calculating power consumption is in the design process of power reduction methods, especially DVFS technique (Huerta, Vasić, Castro, Alou, & Cobos, 2006; Mohan et al., 2010) where the voltage is used to reduce the power consumption of the digital circuit based on the process time.

In the previous chapter, methods that reduce power in digital systems were discussed and DVFS was chosen to be the main power reduction method throughout this thesis. In this chapter, a mathematical model for dynamic power consumption is built so that it can be used in later chapters to measure digital systems power with and without SPM. This chapter will look at the energy in the CMOS circuit so that an accurate power model is built. After that, the new model is to be tested using different digital systems to test its ability to represent dynamic power.

3.2. REVIEWING DYNAMIC POWER MODEL.

When dealing with power reduction, most researchers look at the dynamic power consumption rather than the whole consumed power. This is because dynamic power consumption takes more than 50% of the consumed power (Martin et al., 2002). Furthermore, DVFS method reduces V_{dd} to achieve the required dynamic power reduction that will reduce the overall power since V_{dd} is part of the three types of power consumption discussed in section (2.2). Due to the previous reasons, this thesis will only look at the dynamic power dissipation.

Reviewing equation (2.7), it can be seen that the equation does not correctly describe the dynamic power in digital circuits. In fact, although researchers like Jaeger and Nielson (Jaeger & Blalock, 2008; Nielsen et al., 1994) used this formula to describe power in digital circuits, Ishihara and Pindoo (Ishihara & Yasuura, 1998; Pindoo et al., 2015) used a more realistic equation given by:

$$P_d = \alpha . F . V_{dd}^2 . \sum_{i=1}^{n} C_{Li} \quad (3.1)$$

C_{Li} is the load capacitor of the i^{th} gate in the circuit, and n is the number of gates in the circuit.

Another point mentioned in section (2.3.5) is that there is a relationship between V_{dd} and the frequency. The relation is simply that: the maximum frequency the digital circuit input can use, is inversely proportional with the circuit delay time. The circuit delay time is the sum of all the gates delay in which the input will propagate through to the output. The gate time delay (t_d) is given by (Jaeger & Blalock, 2008; Malhotra, 2015; Piguet, 2006; Sicard, 2003) as:

$$t_d = \frac{C_L . V_{dd}}{\mu . C_{ox} . \frac{W}{l} . (V_{dd} - V_{th})^2} \quad (3.2)$$

where μ is the carrier mobility, C_{ox} is the oxide capacitance, w/l is the transistor width to length ratio, and V_{th} is the threshold voltage.

Looking at the activity factor (α), it was unjustifiably taken as 0.1 by many researchers (Brodersen, Chandrakasan, & Sheng, 1992; Guyot & Abou-samra, 1998). This means that the circuit will produce the same power whatever the change in the inputs. A closer look at the activity factor showed that it is the product of the probability that the output will be in zero state (p_0) in the current clock cycle, multiplied by the probability that the output will be in the one state in the same clock cycle(Rabaey, Chandrakasan, & Nikolic, 2002), ie:

$$\alpha = p_0 . p_1 = p_0 (1 - p_0) \quad (3.3)$$

For a gate that contain N bit inputs, then the activity factor is given as (Rabaey et al., 2002):

$$\alpha = \frac{N_0}{2^N} . \frac{N_1}{2^N} = \frac{N_0 . (2^N - N_0)}{2^{2.N}} \quad (3.4)$$

where N_0 is the number of the zero entries of the input, N_1 is the number of one entries in the input.

For a combinational logic circuit the complexity of equation (3.4) is increased because the probability of each gate should be calculated individually and an overall α is found from the circuit. To summarize, calculating α depends on the input signal rather than the behaviour of the circuit toward the input change (Rabaey et al., 2002) which leads to an accurate calculation of the circuit power.

From the above discussion, it is clear that there is a need for a better model to describe dynamic power dissipation in digital circuits. Yet, before deriving such a model, it is required to find a C_L associated with each gate in the digital circuit.

2.5.1. Load Capacitor (C_L) in digital circuits.

One of the major parameters that affect dynamic power consumption is the load capacitor which, if reduced, will not only reduce the power but also the delay time of the logic gates in the circuit, as seen in equation (3.2). Calculating this parameter is highly dependent on the logic circuit architecture and the technology behind it, as discussed below.

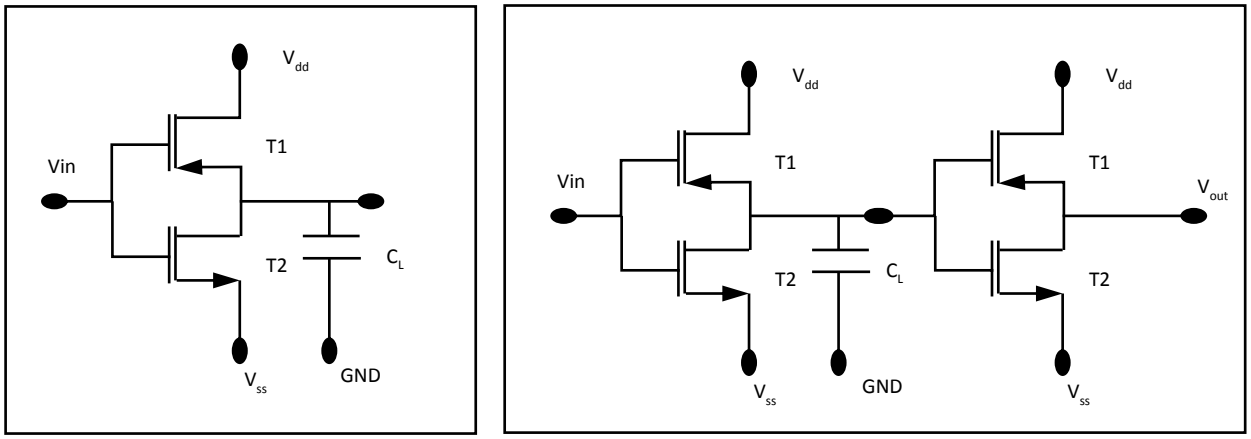
Looking at a CMOS inverter, Figure (3.1.a) (A. Chandrakasan, Bowhill, & Fox, 2001; C. C. Liu, 2007; Piguet, 2006; Schwarz & Oldham, 1993), it can be shown that:

$$C_L = C_{Dp} + C_{Dn} \quad (3.5)$$

Where C_{Dp} is the p substrate drain capacitor and C_{Dn} is the n substrate capacitor.

Equation (3.5) is valid only when the gate is not connected to another gate or load. However, the true case is seen in figure (3.1.b), where the gate is connected to another CMOS gate. Hence, equation (3.5) is modified to accept the input capacitance of the output stage and will become as (Schwarz & Oldham, 1993):

$$C_L = C_{Dp} + C_{Dn} + C_{Gp} + C_{Gn} \quad (3.6)$$



(a) (b)

Figure (3.1): CMOS Circuits: a. CMOS invertor. b. Cascaded Invertor.

C_{Gp} and C_{Gn} are the p and n substrate gate capacitance respectively.

Looking at equation (3.6) thoroughly, and putting into consideration that the logic gate could be connected to more than one gate at the same time, one can deduce the following formula (Jaeger & Blalock, 2008):

$$C_L = C_{Dp} + C_{Dn} + no.\left(C_{Gp} + C_{Gn}\right) \quad (3.7)$$

no. is the fan out (number of connected output gates) of the logic gate.

C_{Gn} and C_{Gp} could be calculated from (Balijepalli, Sinha, & Cao, n.d.; Y. Cao, Sato, Orshansky, Sylvester, & Hu, 2000; Yu Cao, 2011; Zhao & Cao, 2006):

$$C_{Gi} = w_i.\, l_i.\, C_{ox} \quad (3.8)$$

while C_{Dn} and C_{Dp} are given by (Y. (Kevin) Cao, 2006; Yu Cao, 2011; EnOcean, 2011)

$$C_{Di} = C_{Dio}.\, w_i \quad (3.9)$$

i is either n or p and w_i, l_i are the width and the length of the iMOS transistor. C_{Dio} is a constant given according to the used technology.

C_{ox} can be calculated from (Jaeger & Blalock, 2008):

$$C_{ox} = {}^{\varepsilon_{ox}}/_{T_{ox}} \quad (3.10)$$

where ε_{ox} is the permittivity of the oxide and T_{ox} is the thickness of the oxide.

ε_{ox} is given by:

$$\varepsilon_{ox} = 3.9.\varepsilon_0 \quad (3.11)$$

ε_0 is the permittivity of the free space and is equal to $8.854x10^{-12}$ (F/M^2).

Equation (3.7) shows clearly that C_L is dependent on the connectivity of the gate in the logic circuit and on the used technology. Therefore, C_L in a 65nm technology will be bigger than that of a 20nm technology, and hence, the time delay is longer and the power consumption is bigger in 65nm than that of 20nm.

3.3. INVESTIGATION OF ENERGY AND POWER IN CMOS CIRCUITS.

Equation (3.1) gives an estimation of the consumed dynamic power of the gate in the logic circuit regardless of the following parameters: the transistors dimensions, the connectivity of the logic gate in the circuit and the input frequency to the logic gate itself, and hence, its time delay. In the literature, equation (3.1) combines all the previously listed parameters into α which is unjustifiably taken as 0.1 (A. P. Chandrakasan et al., 1992; Chauhan, 2012; Guyot & Abou-samra, 1998). The above-mentioned parameters should be introduced to the power equation so that a better approximation of the power is produced without the need to simulate the circuit at a lower level and complicate the design procedure.

A simple way to derive the power relation of the logic circuit is to sum up the energy produced by each gate in the circuit at a sample time (T) and produce a relation that links the total energy to the behaviour of the circuit and its frequency. Energy produced by a logic gate can be calculated by (Jaeger & Blalock, 2008; Kaczer et al., 2002; Zdebel, 1997):

$$E_i = C_{Li}.V_{dd}^2 \quad (3.12)$$

E_i is the energy associated with the i^{th} gate in the circuit while C_{Li} is the load capacitor associated with the i^{th} gate.

By introducing a factor β_i that represents the activity of the circuit in time (T), the total Energy (E_T) produced by the logic Circuit can be written as:

$$E_T = \sum_{i=1}^{n} \beta_i(k.T)\,.\,C_{Li}.V_{dd}^2 \quad (3.13)$$

n is the number of gates in the circuit, T is the sample time, and k is an integer.

$\beta_i(kT)$ is dependent on both time and the logic behaviour of the gate itself. $\beta_i(kT)$ could be found through the observation of a logic gate behaviour inside a logic circuit and it could be calculated through the following procedure:

Define S_i as the sum of all the i^{th} gate inputs at sample time (kT) or:

$$S_i = \sum_{j=1}^{M_i} I_{i,j}(k.T) \quad (3.14)$$

M_i is the number of inputs of the i^{th} gate, while $I_{i,j}$ is the j^{th} input to the i^{th} gate at time (kT).

Define g_{xi} (S_i) as the function that represents the i^{th} gate behaviour corresponding to its inputs, and its range is [0, 1]. x is the gate type. Since S_i is a time-dependent variable, g_{xi} will also depend on time. Therefore, the gate output can be monitored through time by g_{xi}. Table (3.1) gives the values of g_{xi} corresponding to S_i for different types of gates (x).

Table 3.1: The Value of g_{xi} According to the Gate Type and the Sum of Inputs.

x	$g_{xi}(S_i)$	
	0	1
NOT	S=1	S=0
OR	S=0	S>0
AND	S≠M	S=M
NOR	S>0	S=0
NAND	S=M	S≠M
XOR	S is even	S is odd
XNOR	S is odd	S is even

Gate energy is harvested through observing its output change. By introducing a parameter ch(g_{xi}), the changes of the gate output in the sample time (kT) can be monitored. ch(g_{xi}) is given by:

$$ch_i(g_{xi}) = f\big(g_{xi}(S_i, k.T), g_{xi}(S_i, (k-1).T)\big) =$$
$$\begin{cases} 0; & if\ g_{xi}(S_i, kT) = g_{xi}(S_i, (k-1).T) \\ 1; & if\ g_{xi}(S_i, k.T) \neq g_{xi}(S_i, (k-1).T) \end{cases} \quad (3.15)$$

From equation (3.15) it is seen that any change in the output cannot be seen until the gate time delay t_{di} passes. Hence, β_i(kT) is written as:

$$\beta_i(k.T) = \begin{cases} 0; & ch_i(g_{xi}) = 0\ or\ k.T < t_{di} \\ 1; & ch_i(g_{xi}) = 1\ and\ k.T \geq t_{di} \end{cases} \quad (3.16)$$

Since C_{Li} and β_i are gate related parameters, equation (3.13) can be rewritten after introducing the circuit input frequency F as:

$$P_d = F.V_{dd}^2.\sum_{i=1}^{n} C_{Li}\beta_i(k.T) \quad (3.17)$$

To harvest the energy of a logic circuit, C_{Li} and t_{di} should be found first using equations (3.7) and equation (3.2) respectively for each gate. Then, an initial state to the logic circuit should be set by assuming an initial input and calculating $g_{xi}(0)$ throughout the circuit regardless of the delay time (t_{di}) of the gates. Next, the energy is summed from the logic gates over a

sampling time T<< 1/F. After completing one cycle of frequency, the summed energy is multiplied by F to produce the cycle power, noting that the input is changing in every frequency cycle.

3.3.1. Circuit Time delay.

The time needed for each gate to produce an output is given in equation (3.2). This equation assumes that the gate input is either 1 or that the set of gate inputs are changing at the same time, which is not the case in the logical circuit. Since each gate has its own delay time, number of inputs, and number of outputs, it will be reasonable that the gate output will not settle until the last delayed input arrives and the time delay of the gate itself is reached. Consider $\tau(I_{i,j})$ as the delay of the j^{th} input of i^{th} gate, so the gate output delay could be calculated from:

$$T_{di} = \max\left(\tau\left(I_{i,j}\right)\right) + t_{di} \tag{3.18}$$

The worst-case output time delay or the circuit time delay (T_{max}) is given by:

$$T_{max} = max(T_{dz}) \tag{3.19}$$

where z is an index of all the output gates.

3.3.2. The Proposed Digital Circuit Power Calculation Algorithm.

To calculate the power associated with the circuit activity for a certain input, two stages should be considered. The first is calculating the load capacitor for each gate individually according to equations (3.7) -(3.11) and according to the connectivity of the circuit. The second stage is to traverse the behaviour of the circuit through time toward its input, putting in mind that every set of inputs could produce different power consumption according to the functionality of the circuit itself. The algorithm for calculating the dynamic power is as follows:

The initialization stage:

1. Set the initial parameters of the design according to table (3.2) (Sinha et al., n.d.; Zhao & Cao, 2006).
2. Calculate C_{ox} according to equation (3.10).
3. For each gate in the circuit, calculate C_{Li} according to equations (3.7)-(3.9).
4. For each gate in the circuit, calculate t_{di} according to equation (3.2) and substituting C_L with the value of C_{Li}.

Figure (3.3) shows the traversing algorithm flowchart.

This algorithm was tested with different conditions to find the effect of the parameters on the consumed power of the logic circuit. The tests and their results are discussed in the next section.

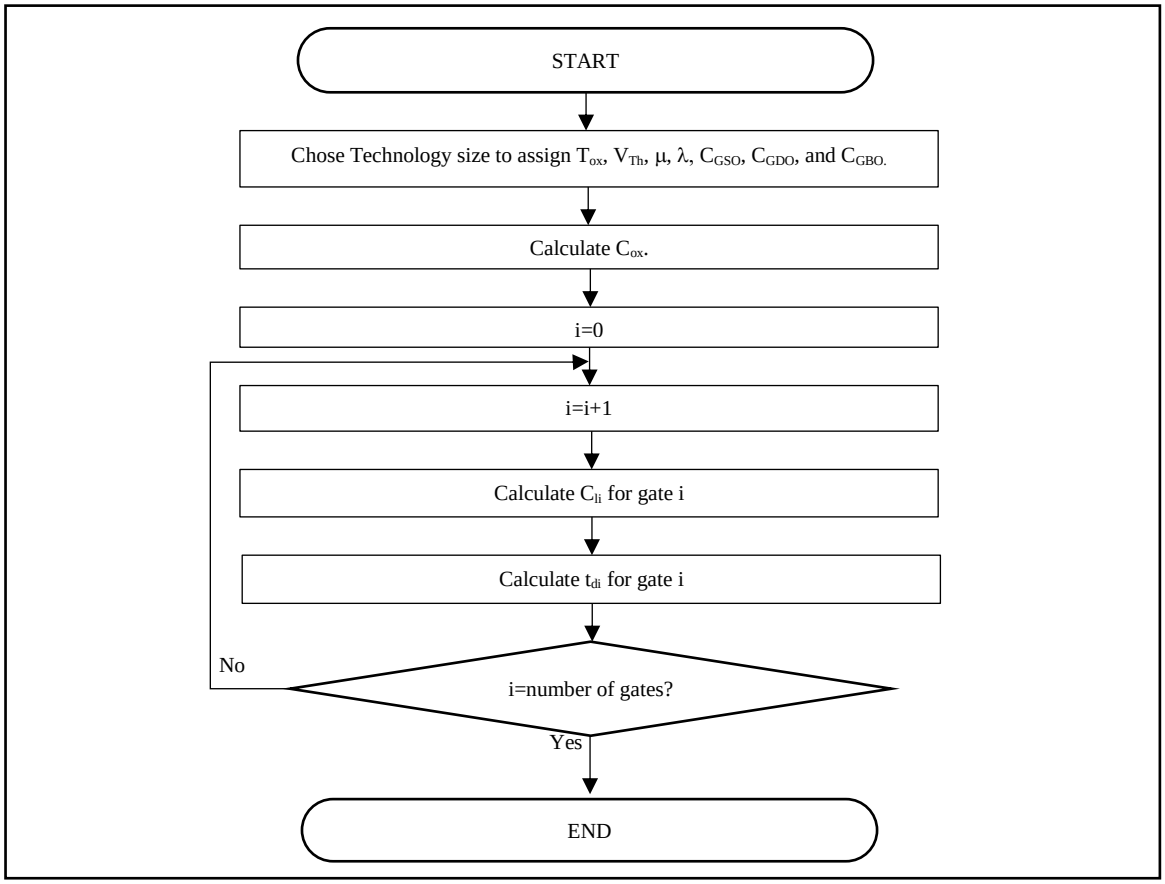


Figure 3.2: The Initialization Phase of the Proposed Algorithm.

The initialization phase flowchart is shown in Figure (3.2).

Table 3.2: Used Parameters (Sinha et al., n.d.; Zhao & Cao, 2006).

Used Technology	Transistor Type	T_{ox} (nm)	V_{Th} (V)	μ (m^2/V.S)	λ	C_{GSO} (F)	C_{GDO} (F)	C_{GBO} (F)
180n	pMOS	4.2×10^{-9}	-0.42	8×10^{-3}	2	0.2786×10^{-9}	0.2786×10^{-9}	25.6×10^{-12}
	nMOS	4×10^{-9}	0.3999	35×10^{-3}	0.05	0.2786×10^{-9}	0.2786×10^{-9}	25.6×10^{-12}
90n	pMOS	2.15×10^{-9}	-0.339	0.00711	0.12	0.18×10^{-9}	0.18×10^{-9}	25.6×10^{-12}
	nMOS	2.05×10^{-9}	0.397	0.0547	0.06	0.19×10^{-9}	0.19×10^{-9}	25.6×10^{-12}
45n	pMOS	1.3×10^{-9}	-0.49158	0.02	0.12	0.11×10^{-9}	0.11×10^{-9}	25.6×10^{-12}
	nMOS	1.25×10^{-9}	0.46893	0.054	0.02	0.11×10^{-9}	0.11×10^{-9}	25.6×10^{-12}
22n	pMOS	1.1×10^{-9}	-0.4606	0.0095	0.12	65×10^{-12}	65×10^{-12}	25.6×10^{-12}
	nMOS	1.05×10^{-9}	0.50308	0.04	0.02	65×10^{-12}	65×10^{-12}	25.6×10^{-12}

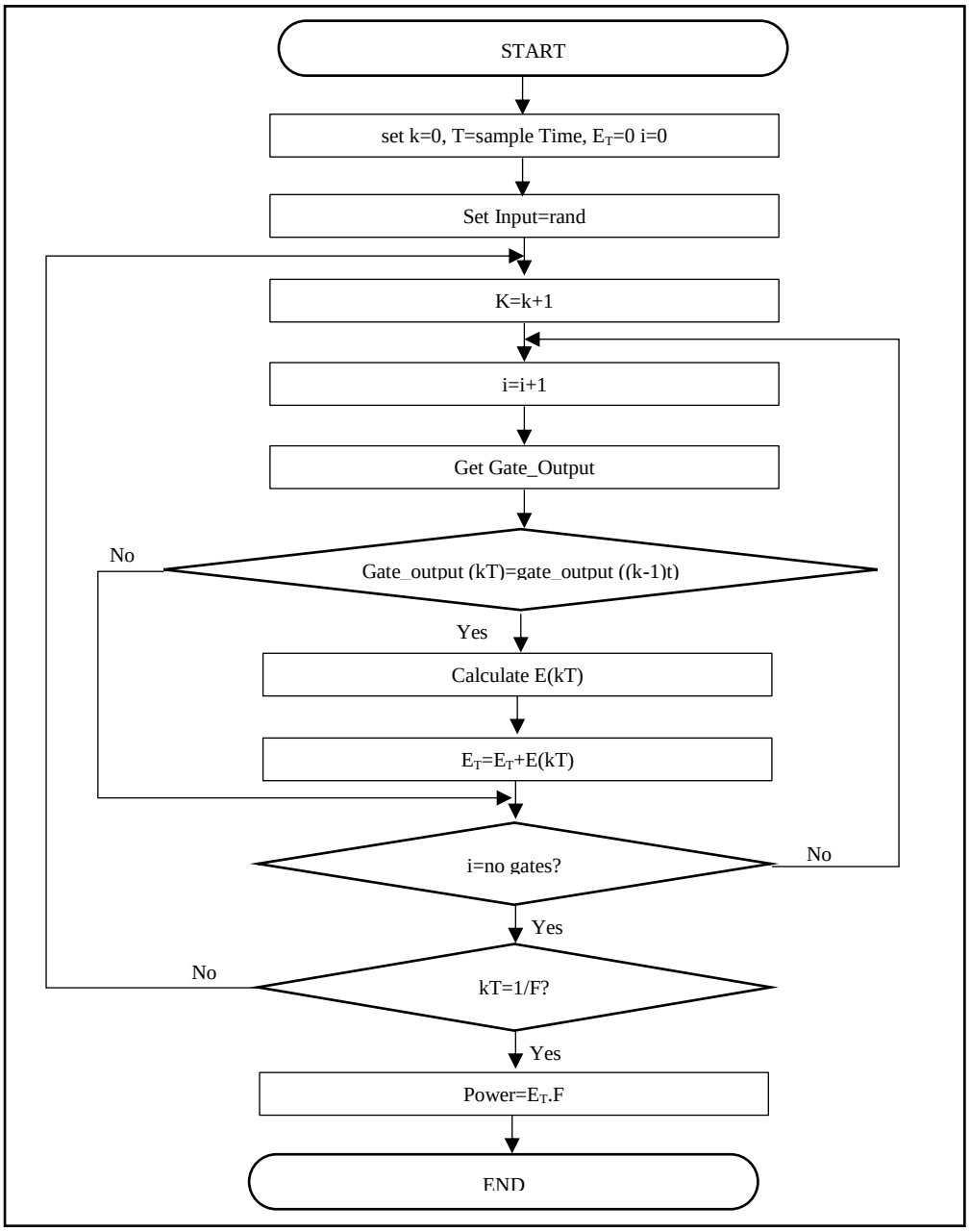


Figure (3.3): The Traversing Phase of the Proposed Algorithm.

The Traversing stage:

Before applying this algorithm, an initial state of the logic circuit should be set by assuming an initial input and calculating $g_{xi}(0)$ for each gate regardless of the delay time (t_{di}) of the gate.

The traversing algorithm will work for each input set governed by F. It assumes a sampling time T<< 1/F so that the glitch effect is observed thoroughly. The algorithm is given by:

1. Produce random input sets for the circuit.

2. Set E(t)=0.
3. Set t=kT.
4. Find each gate output and energy E(t) corresponding to the current input set and according to equation sets (3.12) and (3.15) -(3.17).
5. $E_T(kT)=E_T((k-1)\ T)+E(kT)$.
6. If $kT \neq 1/F$, repeat steps 1-5
7. Change the input set, set k=k+1, repeat from 1 until the whole input set is empty.
8. Find the average of the dissipated power for the entire input set.

The traversing phase flowchart is presented in Figure (3.3).

It is worth noting that in step 2 it is not necessary that the chosen random input produces the required dynamic power of the circuit. Hence, a number of these inputs are used and the average power is used to represent the dynamic power. After trying 10, 100, 500, 1000, 2000, and 5000 random inputs, the average power calculated for different circuits withstand no significant change after the 1000 random inputs. So it was seen from the experiments that 1000 randomly chosen inputs can represent the dynamic power of the circuit accurately.

3.4. VERIFICATION OF POWER DISSIPATION MODEL.

Equation (3.17) managed to describe the relations between voltage, frequency, time delay of the gates, transistors size, and gates connections with the dynamic power. To prove this relation, series of tests were made with different logic circuits under different conditions. The tests were carried out using OrCAD Cadence for simulating the CMOS transistor circuits and to record their power. On the other hand, MATLAB was used to implement the power dissipation algorithm on the digital circuits so that the circuit power is calculated. The circuits used in this test are:

1. The CMOS Invertor (NOT gate).
2. The 2×1 Multiplexer.
3. One-bit Full Adder (FA).
4. Two-bit FA.

Choosing these circuits did not come from the void. The NOT gate is the norm of the CMOS circuits. The 2×1 Multiplexer and one-bit FA are the basic building blocks of the microprocessor circuits. The two-bit FA was chosen to show the ability of the power reduction model to produce accurate reading of power regardless of the number of the circuit inputs.

Before introducing the test results, it is wise to show how OrCAD Cadence simulate CMOS circuits and how it calculates the dynamic power.

3.4.1. Using OrCAD Cadence to Simulate Dynamic Power in CMOS Circuits.

OrCAD Cadence utilises PSpice and Advanced Analysis technology to associate industry-leading, analogue, mixed-signal, and analysis engines to produce a complete circuit simulation and verification solution ("Overview Page - OrCAD PSpice Designer | OrCAD," n.d.). It uses the BSIM as a base to simulate the electronic devices (Morshed & Berkeley, n.d.). The method of measuring the dynamic power of the CMOS circuits was based on ("Overview Page - OrCAD PSpice Designer | OrCAD," n.d.; Wallace, n.d.). It consists of the following steps:

1. Building the circuit and assigning the right parameters to the transistor Spice model (Table 3.2).
2. For every input combination, fix the input and produce the output file for a certain interval of time, and then calculate the power.
3. Find the average static power of the circuit by taking the average of the calculated powers in step 2.
4. Run the circuit under variable inputs for the same time interval chosen in step two, and calculate the power.
5. Find the dynamic power by subtracting the power found in step 2 from that obtained in step 4.

It can be seen from the above steps that to calculate the power of a logic circuit, one should produce (2^n+1) files. n is the number of the circuit inputs. Another important point in these steps is the time of simulation mentioned in step two. If the simulation is for 10MHz input, then it must run for 0.1μs. So for every voltage and frequency point drawn on the graphs there are (2^n+1) files to calculate the dynamic power. For the 2 bit FA circuit, the number of files for each point were 33. Since there were 17 frequency points, 7 V_{dd} points, and the test used 4 technology sizes, the total number of files to be processed was 33×17×7×4 which is equal to 15708. For a circuit of 6 inputs the number of files to be processed is equal to 30940 which makes this process inapplicable if the circuit number of inputs is high.

3.4.2. CMOS NOT Gate.

The NOT gate is the simplest gate in the logic circuits. Its implementation in CMOS requires only two FET transistors of the n and p type. The circuit configuration and the logic symbol of the NOT gate is shown in Figure (3.4) (Jaeger & Blalock, 2008; Kaczer et al., 2002).

The NOT gate CMOS circuit was implemented using OrCAD Cadence and MATLAB to verify the integrity of the proposed power dissipation model. The tests were carried out to show the relations between power and frequency under different voltages and technology sizes. The used technology sizes are (180, 90, 45, 22) nm while the voltages are (0.6, 1, 1.5, 2, 2.5, 3, 3.5) V. It is worth noting that the nominal supply voltages of the given technology sizes are less than 3.5V, but in some circuits there is a need to increase the supply voltage so that the circuit delay time is decreased, enabling the circuit to withstand high frequency.

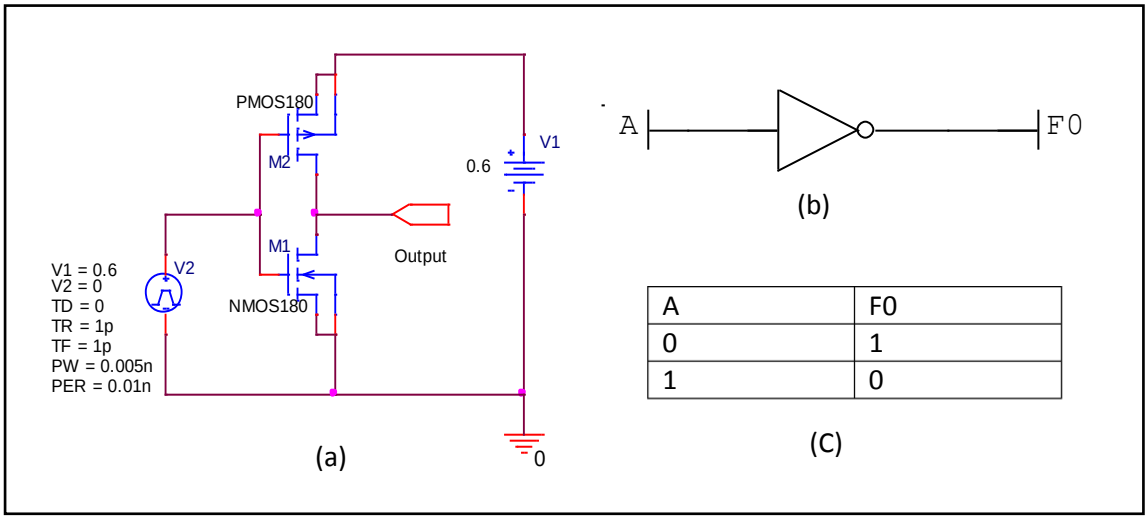


Figure (3.4) CMOS NOT Gate: a. Circuit Diagram. b. Logic Symbol. c. Truth Table.

The dynamic power consumption vs the frequency for an 180nm NOT gate is shown in figure (3.5). The test was carried out using the new power model and different supply voltages. Figure (3.6) shows the dynamic power of the same NOT gate but using OrCAD Cadence. Finally, Figure (3.7) shows the maximum delay time of the NOT gate under different voltages for the new model compared to the maximum time that was calculated using OrCAD Cadence.

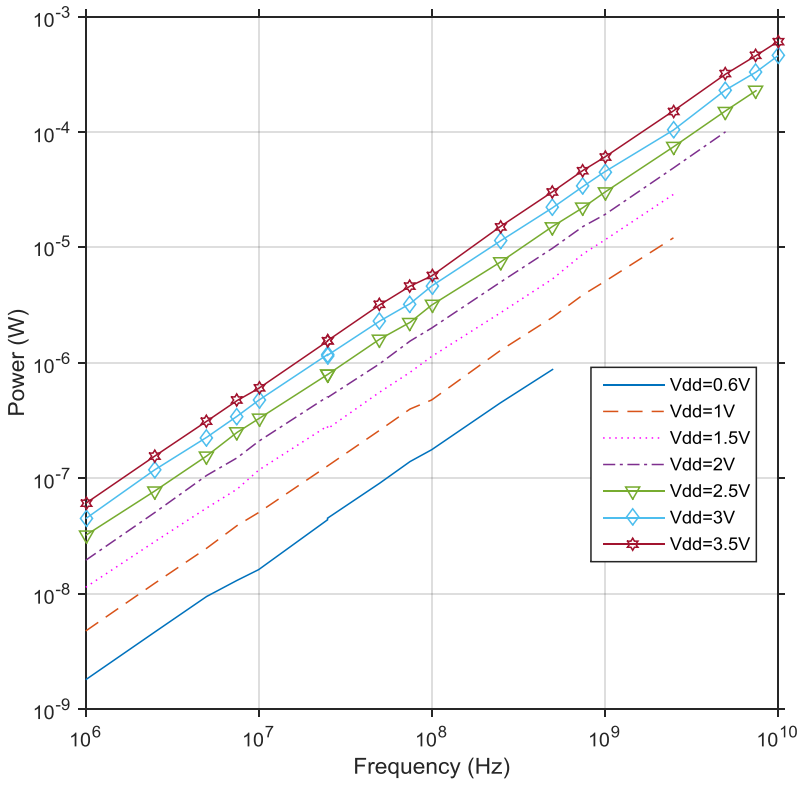


Figure (3.5): Dynamic Power Dissipation Vs Frequency of 180nm NOT Gate Using the Power Model.

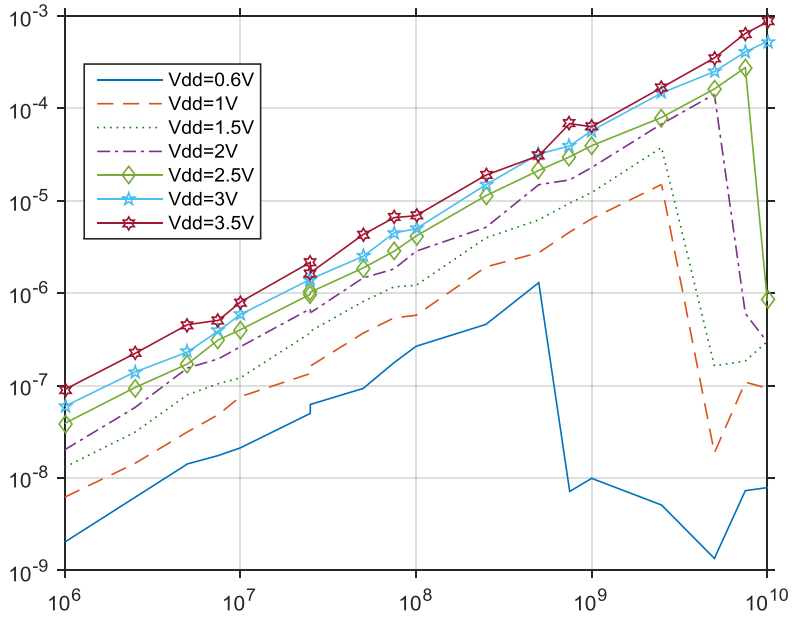


Figure (3.6): Dynamic Power Dissipation Vs Frequency of 180nm NOT Gate Using the OrCAD Cadence.

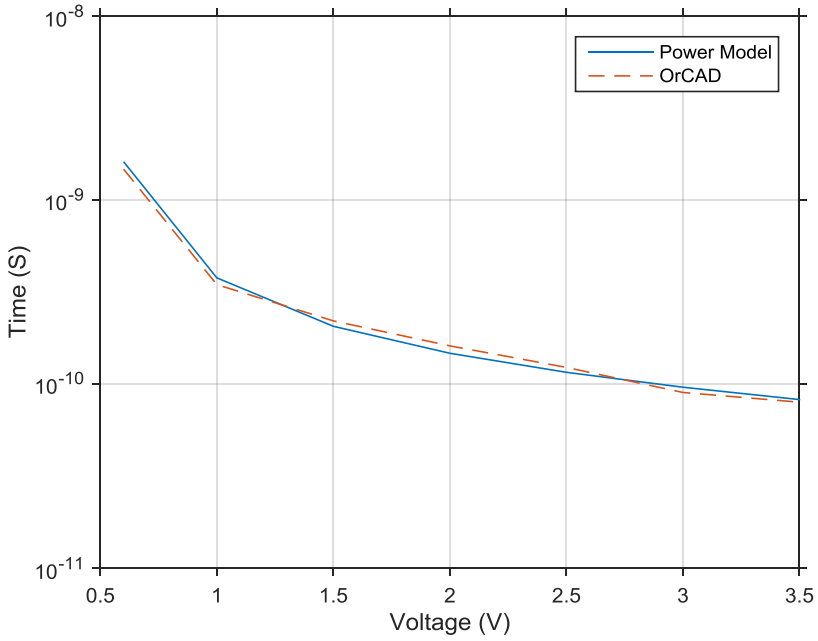


Figure (3.7): Time Delay of 180nm NOT Gate Using the Power Model and OrCAD Cadence.

The simulation results of a 90nm NOT gate are shown in Figures (3.8) for the new power model, figure (3.9) for the Cadence Power measurements, and figure (3.10) for the maximum circuit time delay measured in both the new power model and Cadence.

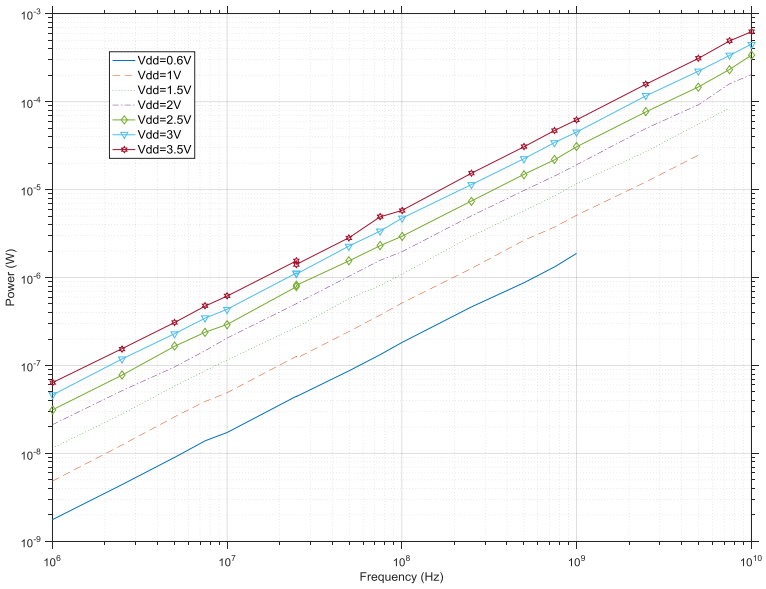


Figure (3.8): Dynamic Power Dissipation Vs Frequency of 90nm NOT Gate Using the Power Model.

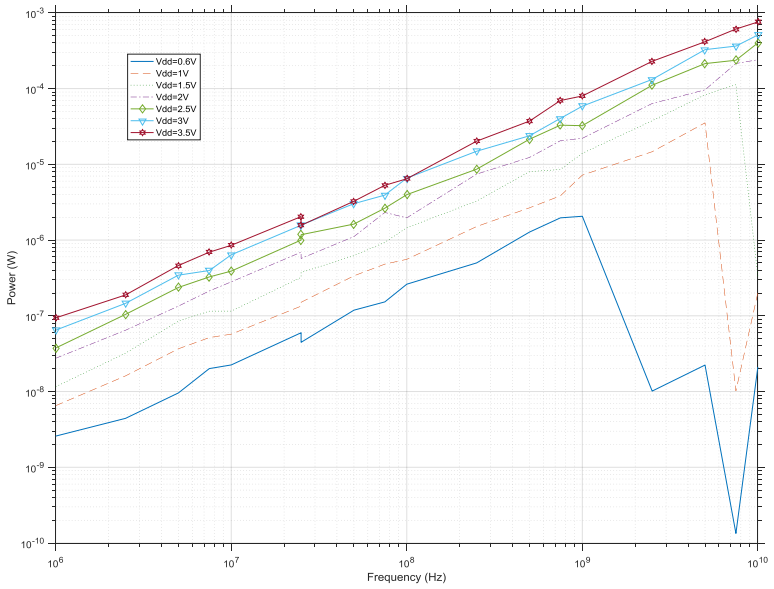


Figure (3.9): Dynamic Power Dissipation Vs Frequency of 90nm NOT Gate Using the OrCAD Cadence.

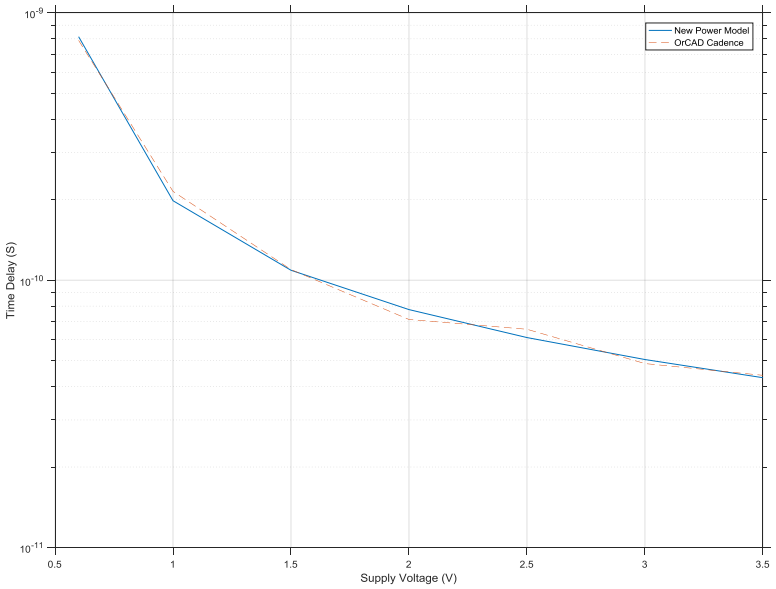


Figure (3.10): Time Delay of 90nm NOT Gate Using the Power Model and OrCAD Cadence.

The simulation results of a 45nm NOT gate are presented in Figures (3.11) for the new power model, figure (3.12) for the Cadence Power measurements, and figure (3.13) for the maximum circuit time delay measured in both the new power model and Cadence.

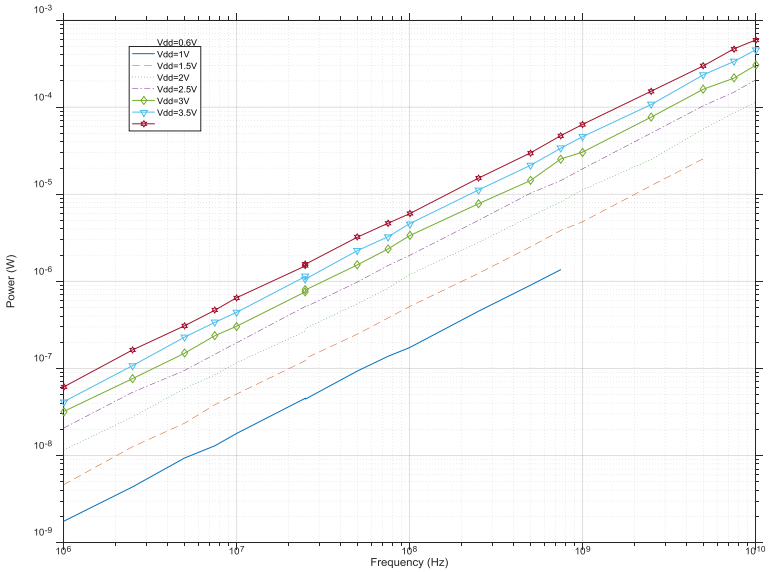


Figure (3.11): Dynamic Power Dissipation Vs Frequency of 45nm NOT Gate Using the Power Model.

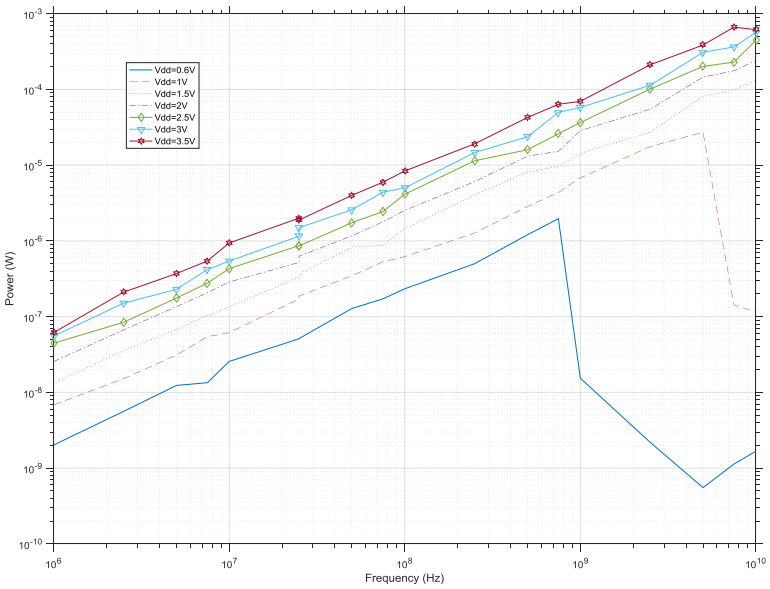


Figure (3.12): Dynamic Power Dissipation Vs Frequency of 45nm NOT Gate Using the OrCAD Cadence.

The simulation results of a 22nm NOT gate are shown in Figures (3.14) for the new power model, figure (3.15) for the Cadence Power measurements, and figure (3.16) for the maximum circuit time delay measured in both the new power model and Cadence.

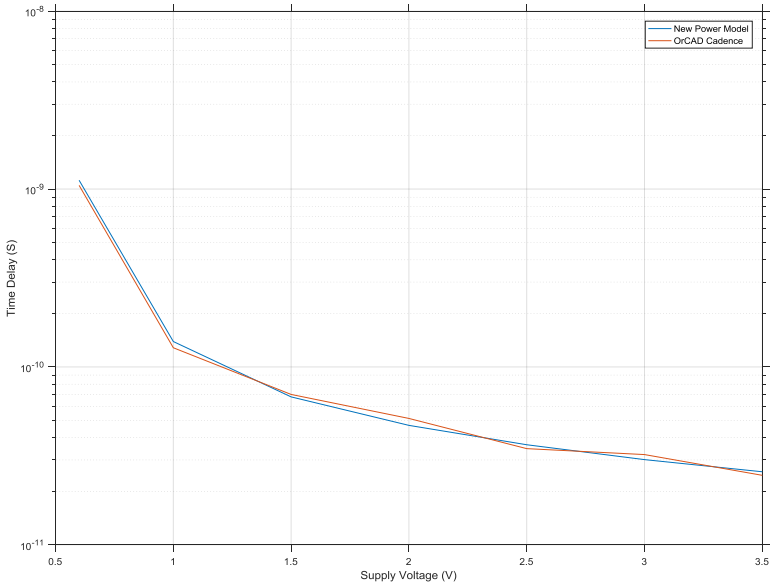


Figure (3.13): Time Delay of 45nm NOT Gate Using the Power Model and OrCAD Cadence.

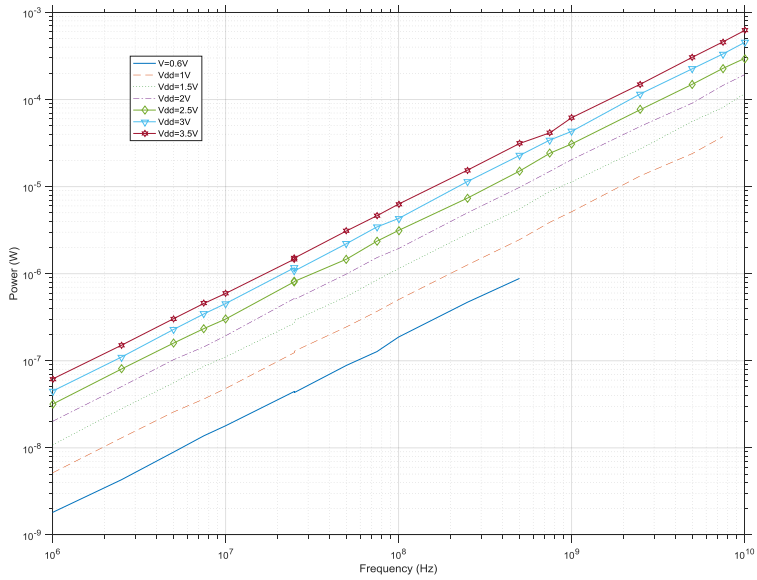


Figure (3.14): Dynamic Power Dissipation Vs Frequency of 22nm NOT Gate Using the Power Model.

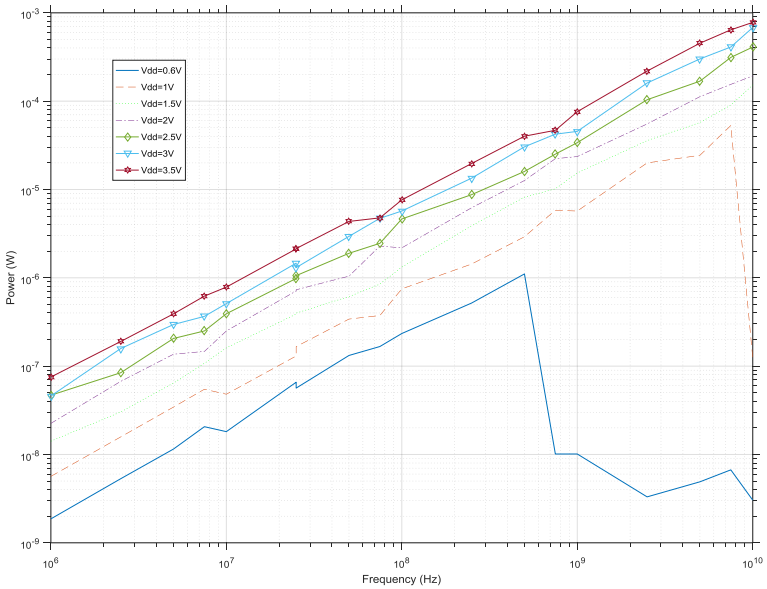


Figure (3.15): Dynamic Power Dissipation Vs Frequency of 22nm NOT Gate Using the OrCAD Cadence.

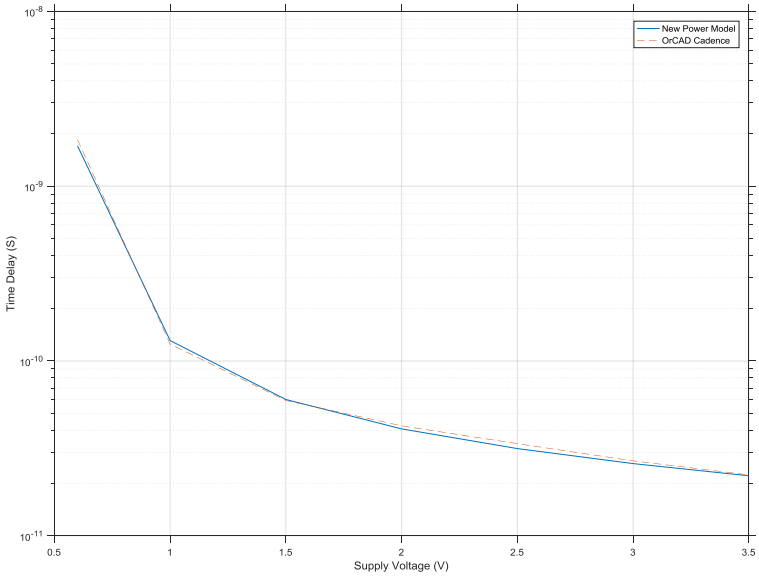


Figure (3.16): Time Delay of 22nm NOT Gate Using the Power Model and OrCAD Cadence.

It can be seen from the Figures above that the power obtained from the new power model is very close to that of the one calculated using OrCAD Cadence. Another important thing to be observed from the figures is that the simulation of the NOT gate using the new power model does not produce any power in some points. Figure (3.5) confirms this observation for the 2.5V and frequencies bigger than 7.5GHz, 2V and frequencies bigger than 5GHz, 1.5V and frequencies bigger than 2.5Ghz, 1V and frequencies bigger than 2.5GHz, and also 0.6V

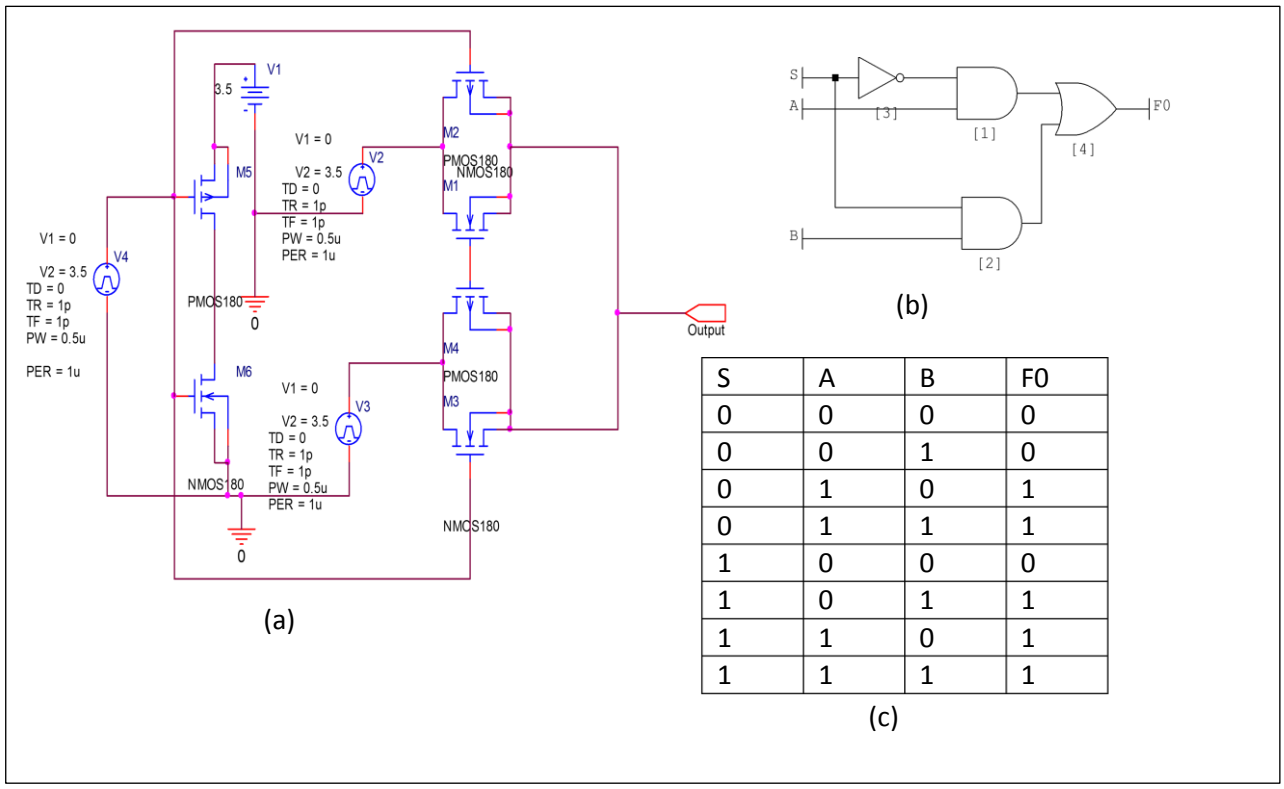
and frequencies bigger than750MHz. This comes from the fact that the gate will not produce an accurate output at high frequencies due to the time delay discussed in section (3.3.1). The value of the power in the new power model in the previously listed intervals is zero since the circuit will not produce any output for the (voltage, frequency) pair used in this point of simulation. This behaviour is also recognized in the OrCAD Cadence simulation. Instead of producing zero as an output, Cadence shows that there are some dynamic power dissipated in the circuit due to the fact that the transistor will not stop working at this point but will produce a voltage less than the threshold voltage. Hence, it will not be considered as a transition between 0 and 1. Another look at the simulation through Figures (3.5), (3.8), (3.11), and (3.14) shows that, as the technology size decreases, the power, as well as the time delay, decreases. This means that choosing a lower technology size will ensure a better power consumption and a higher frequency operation.

3.4.3. CMOS 2×1 MUX.

The multiplexer circuit is widely used in most of the microprocessor circuits and in digital communication systems because it gives the designer the ability to choose between different numbers of inputs. The circuit symbol, circuit diagram, and the truth table of the 2×1 MUX are shown in Figure (3.17) (Pedroni, 2008; Teubner & Woods, 2013).

Figures (3.18) and (3.19) show the 180nm MUX power using the new power model and OrCAD Cadence respectively, while Figure (3.20) shows the maximum delay time of the circuit.

The dynamic power consumption of the 90nm MUX is shown in Figures (3.21) and (3.21). The time delay is presented in figure (3.22).



S	A	B	F0
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(c)

Figure (3.17) CMOS 2×1 MUX: a. Circuit Diagram. b. Logic Symbol. c. Truth Table.

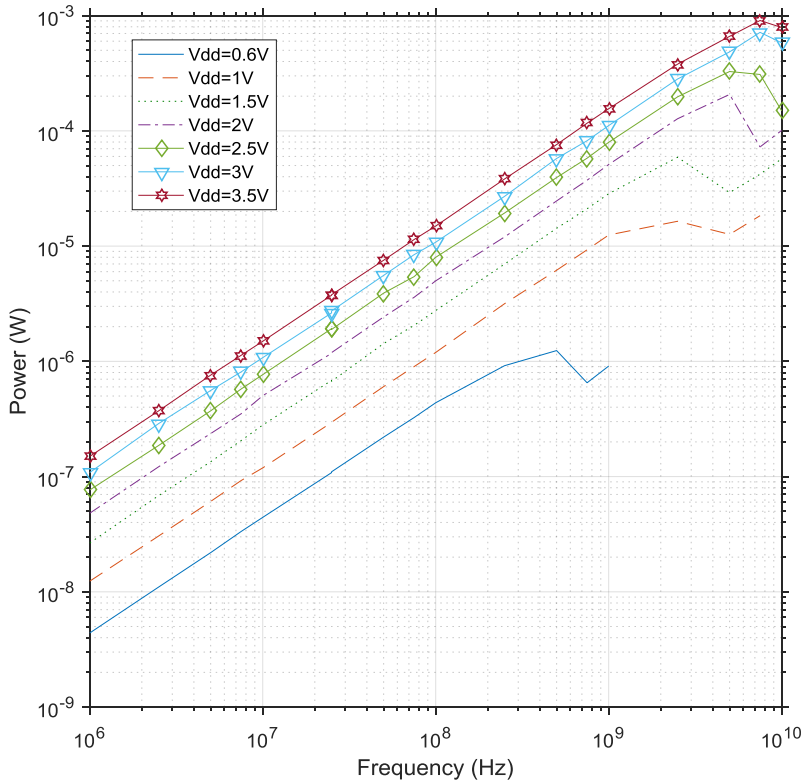


Figure (3.18): Dynamic Power Dissipation Vs Frequency of 180nm 2×1 MUX Using the Power Model.

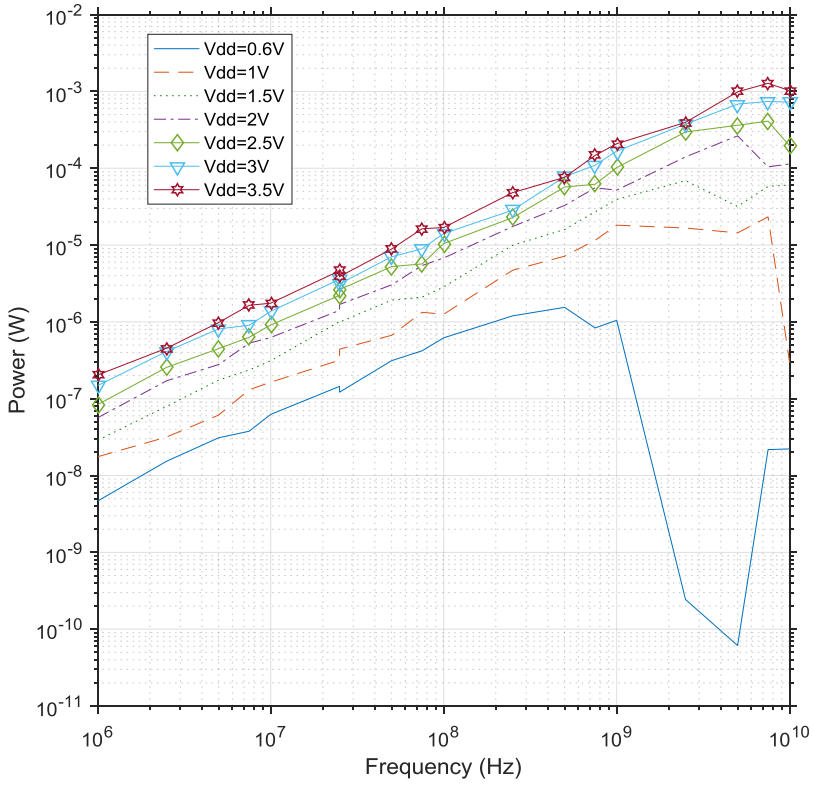


Figure (3.19): Dynamic Power Dissipation Vs Frequency of 180nm 2×1 MUX Using the OrCAD Cadence.

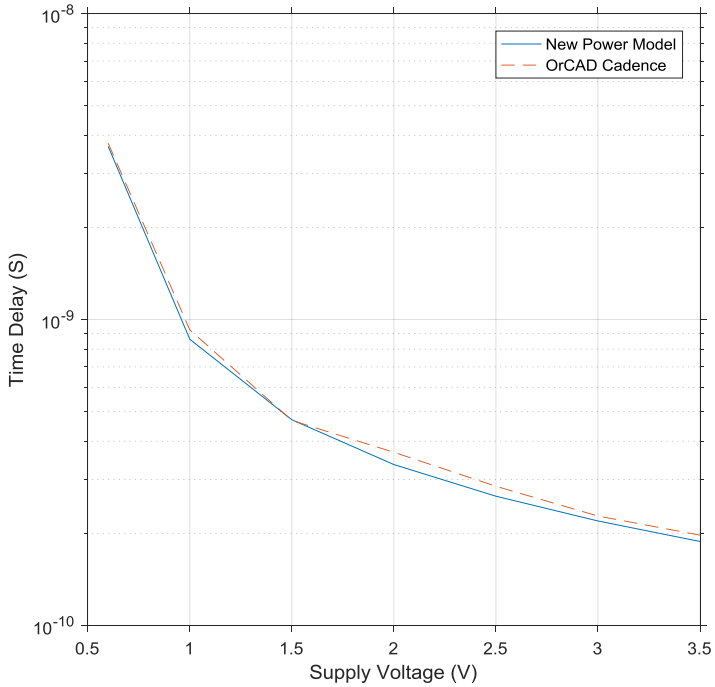


Figure (3.20): Time Delay of 180nm 2×1 MUX Using the Power Model and OrCAD Cadence.

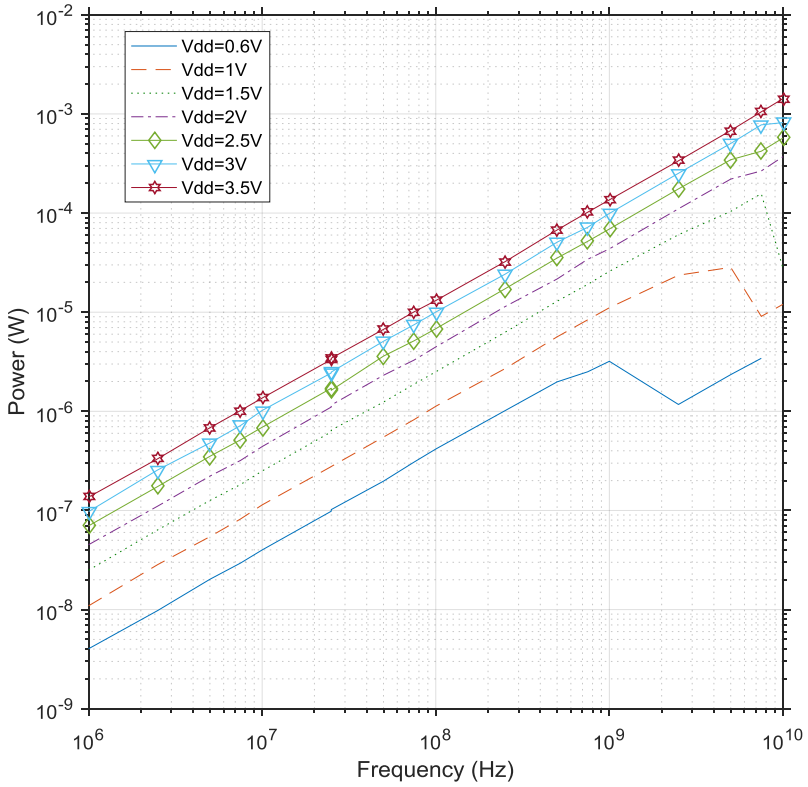


Figure (3.21): Dynamic Power Dissipation Vs Frequency of 90nm 2×1 MUX Using the Power Model.

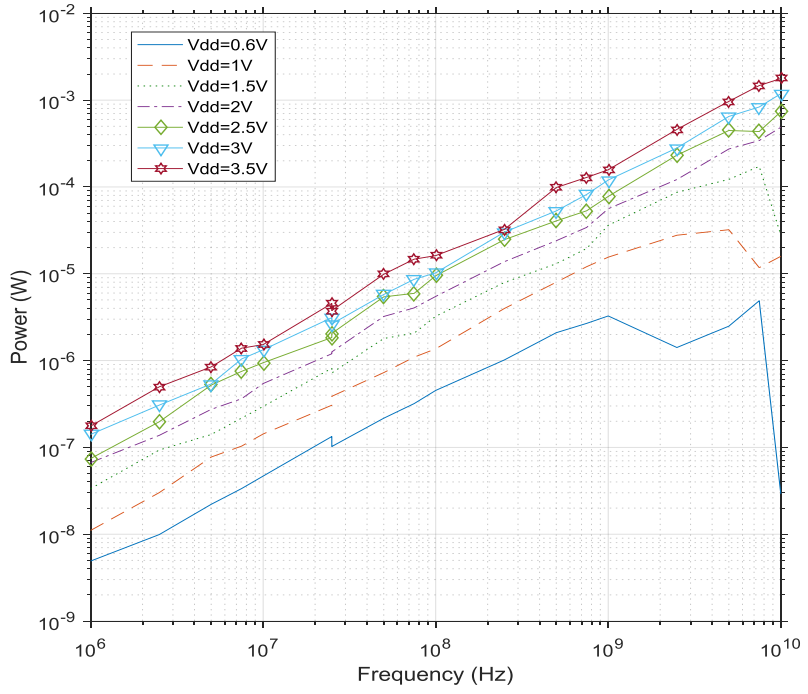


Figure (3.22): Dynamic Power Dissipation Vs Frequency of 90nm 2×1 MUX Using the OrCAD Cadence.

Figures (3.22) and (3.23) show the dynamic power dissipation of the 45nm MUX, while Figure (3.24) shows the delay time of the MUX. Finally, Figures (3.25), (3.26), and (3.27) show the simulation results of the 22nm MUX.

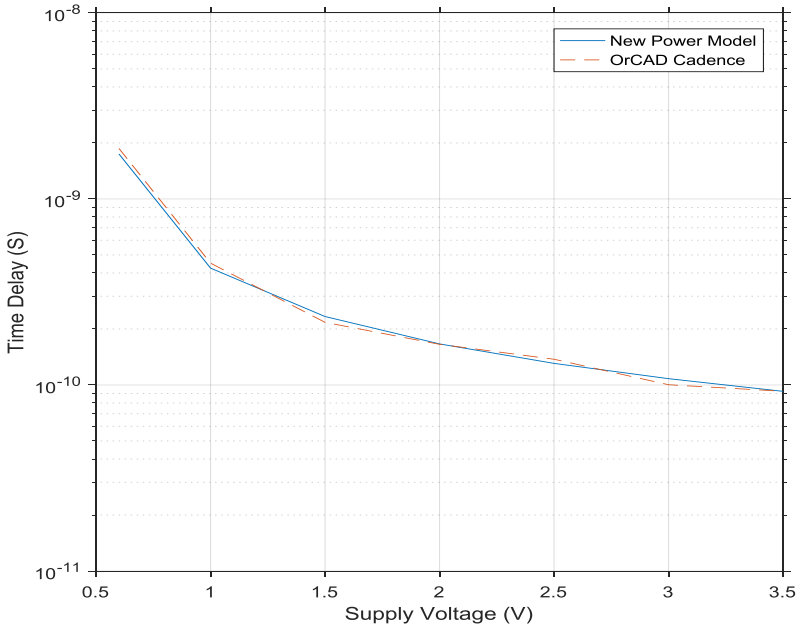


Figure (3.23): Time Delay of 90nm 2×1 MUX Using the Power Model and OrCAD Cadence.

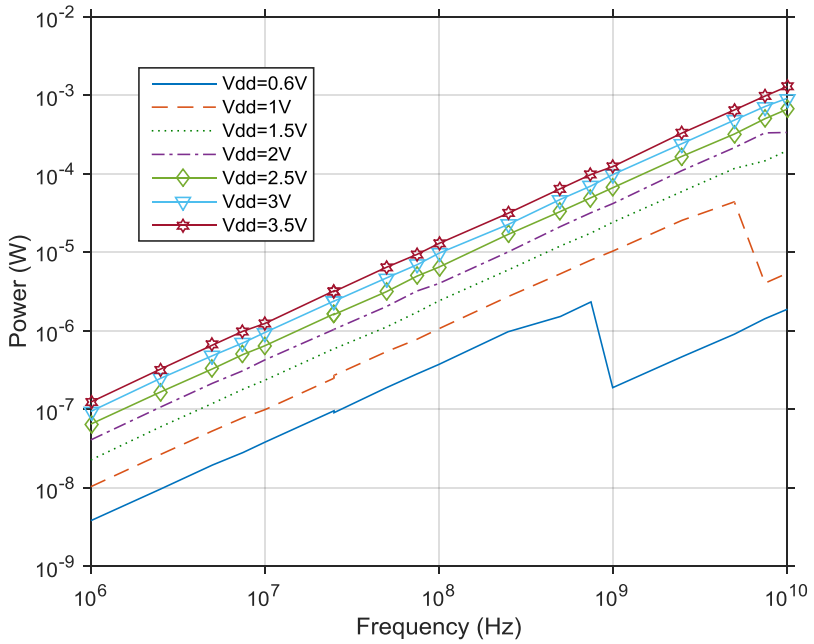


Figure (3.24): Dynamic Power Dissipation Vs Frequency of 45nm 2×1 MUX Using the Power Model.

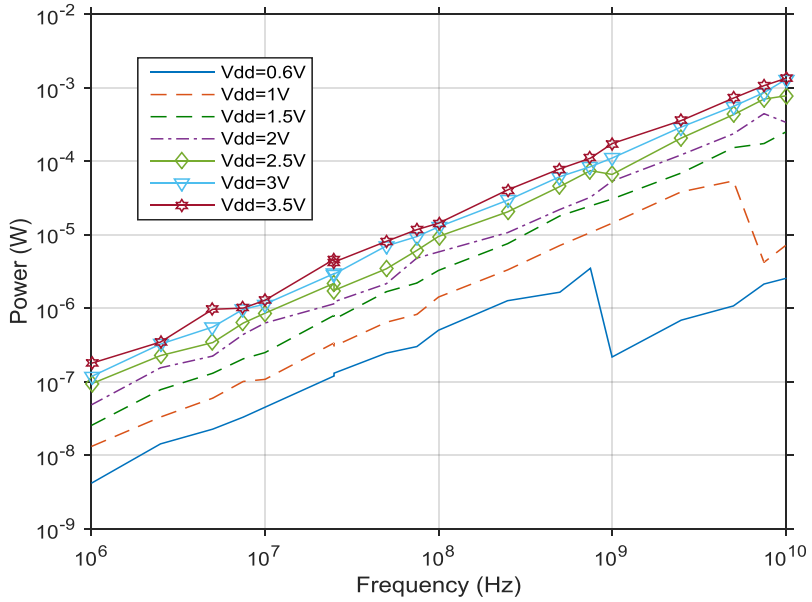


Figure (3.25): Dynamic Power Dissipation Vs Frequency of 45nm 2×1 MUX Using the OrCAD Cadence.

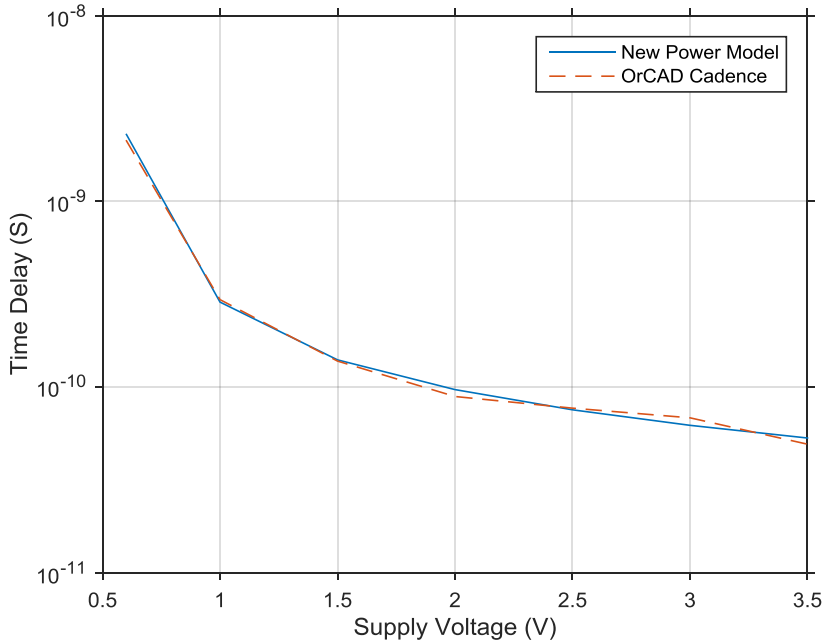


Figure (3.26): Time Delay of 45nm 2×1 MUX Using the Power Model and OrCAD Cadence.

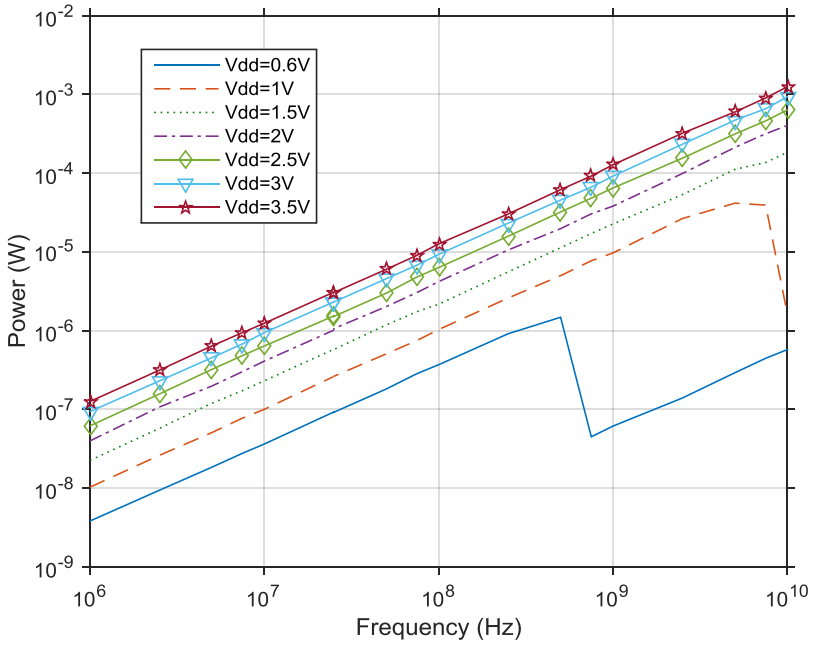


Figure (3.27): Dynamic Power Dissipation Vs Frequency of 22nm 2×1 MUX Using the Power Model.

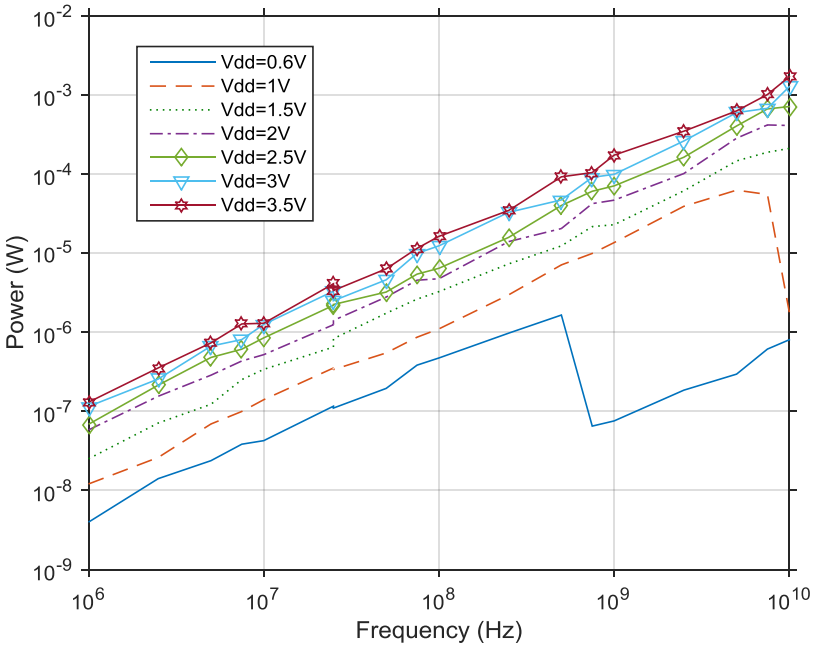


Figure (3.28): Dynamic Power Dissipation Vs Frequency of 22nm 2×1 MUX Using the OrCAD Cadence.

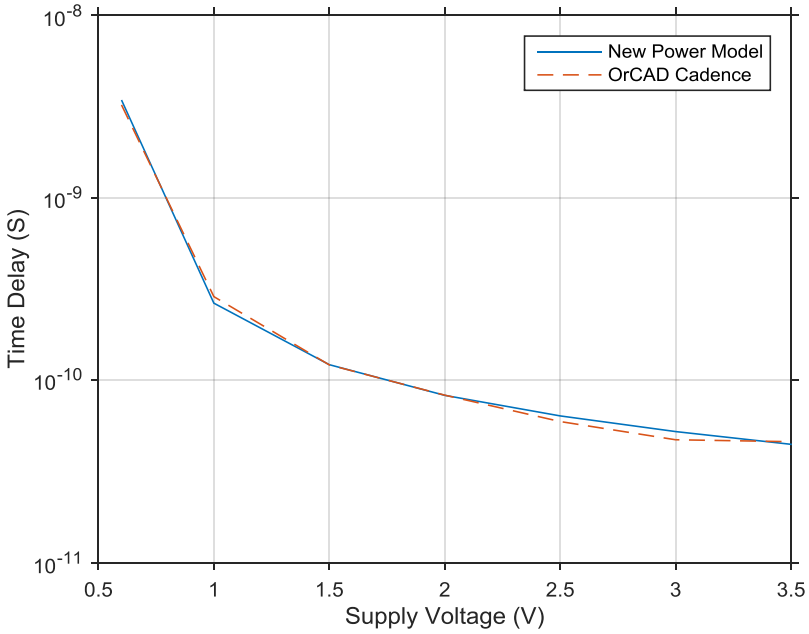


Figure (3.29): Time Delay of 22nm 2×1 MUX Using the Power Model and OrCAD Cadence.

The results of this test are similar to that of the NOT gate. For the 180nm circuit, the power decreases after 750 MHz for a supply voltage of 0.6 (Figure (3.18)), but it starts to increase again after 1GHz to reach its final appearance in 2.5GHz, and then reduces to zero. This behaviour occurs because in high frequency, since the gates are cascaded, some of them will produce a delayed output. The gates after them will receive this delayed output and wait for the delay time to produce an output. Hence, the power is not zero because some of the circuit gates are still receiving faulty inputs and produce output. The increase in power in the region between 1GHz and 2.5GHz is a natural behaviour of the gates toward the frequency. Yet, after 2.5GHz, no gate can withstand the high frequency and will not sense the input changes, which in turn leads to them not producing any output. Thus, power is zero. This effect is shown in the new power model in Figures (3.18), (3.21), (3.24), and (3.27). The behaviour is supported by the OrCAD Cadence simulation in Figures (3.19), (3.22), (3.25), and (3.27).

The high frequency behaviour is improved when using lower technology size. This can be seen from the previous figures where in the 180nm, the circuit cannot work with 10GHz frequency and produce an accurate output. On the other hand, in the case of 90nm the circuit can reach the 10GHz barrier if V_{dd} is 3.5. For a lower technology size, this barrier is overtaken for a lower supply voltage of 2.5V for the 45nm and 1.5V for the 22nm.

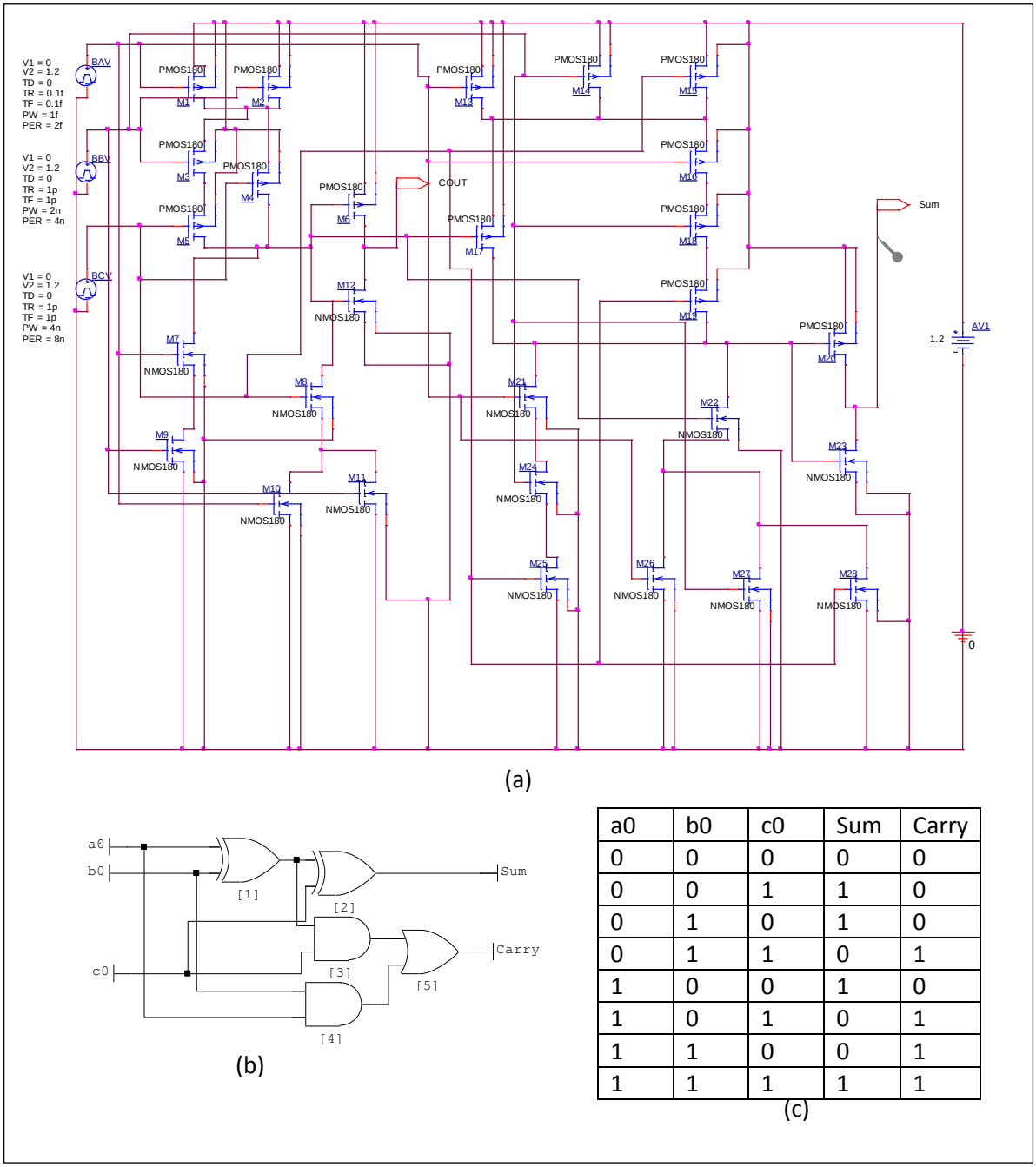
3.4.4. One Bit Full Adder (FA).

The Full Adder (FA) circuit is one of the most widely used circuits in arithmetic digital circuits. It is found in the General Purpose Processors as well as DSP processors. The CMOS and the logic circuits are shown in Figure (3.30) with the truth table for both the Sum and Carry outputs of the circuits.(Manjunath K M, Abdul Lateef Haroon P S, Pagi, & Ulaganathan J, 2015)

The simulation of the FA circuit was carried out using both MATLAB and OrCAD Cadence to prove the ability of the new power model to simulate the dynamic power of different logic circuits. Figures (3.31) and (3.32) show the power results of the new power model and that of the CMOS representation using Cadence. The technology size used in this test is 180nm. The time delay of the circuit is shown in Figure (3.33).

The power dissipation of a 90nm one-bit FA circuit is shown in Figures (3.34) and (3.35). The time delay is shown in Figure (3.36). The 45nm FA circuit results are shown in Figures (3.37), (3.38), and (3.39). Finally, Figures (3.40), (3.41) and (3.42) present the results of the 22nm FA circuit simulations.

The 1-bit FA circuit has only five gates. That brings it very close to the 2×1 MUX which has 4 gates. However, the power behaviour of the circuit is different. It can be seen from Figure (3.18) that the MUX circuit starts to lose its ability to produce an accurate output at 750GHz for 0.6V. Figure (3.31) shows that the FA circuit loses this ability at 500MHZ due to the difference in gate connectivity. In the F A circuit, the gates have more fan out than that of a MUX circuit. Consequently, it could be conclude that the power behaviour of the circuit depends on its architecture. Since this fact is clear even in the OrCAD Cadence simulation (Figures (3.32), (3.35), (3.38), and (3.41)), the superiority of the new power model over the old one, which did not include the connectivity of the gates in the circuit as parameter in the power equation, becomes quite clear. Other Figures prove what was mentioned earlier in section 3.4.3 about how the power acts in a digital circuit with cascaded gates. Again, the relation between the technology size and the power is the same; i.e. as the technology size decreases, the power and the time delay decreases.



a0	b0	c0	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(c)

Figure (3.30) CMOS One Bit Full Adder: a. Circuit Diagram. b. Logic Symbol. c. Truth Table.

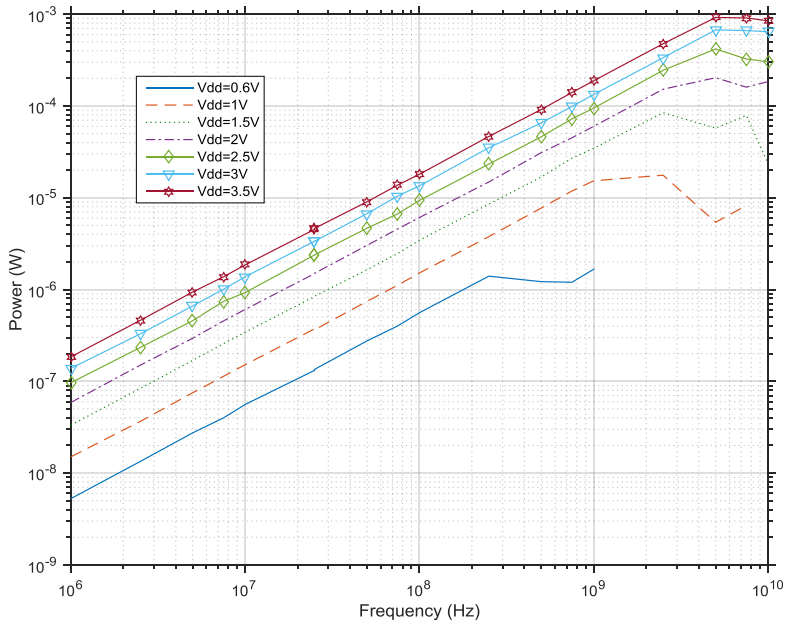


Figure (3.31): Dynamic Power Dissipation Vs Frequency of 180nm 1-Bit FA Using the Power Model.

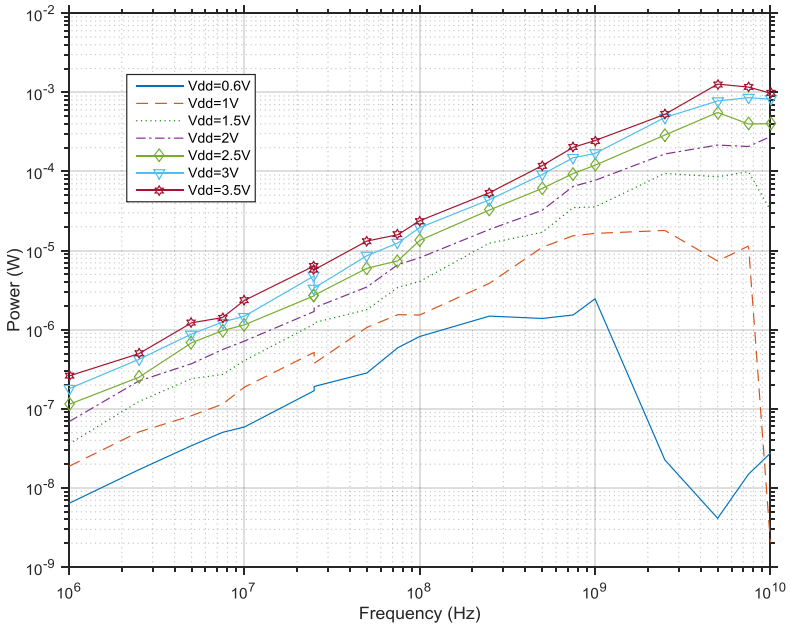


Figure (3.32): Dynamic Power Dissipation Vs Frequency of 180nm 1-Bit FA Using the OrCAD Cadence.

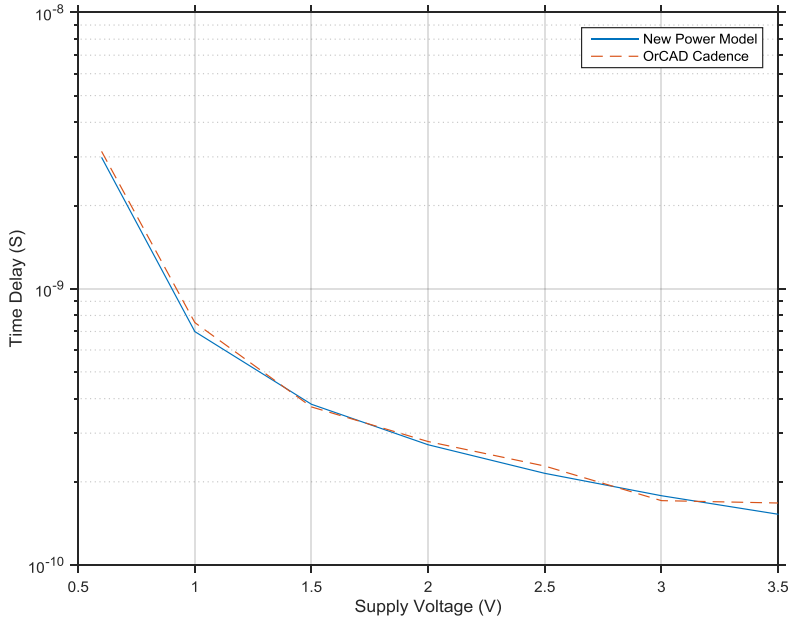


Figure (3.33): Time Delay of 180nm 1-Bit FA Using the Power Model and OrCAD Cadence.

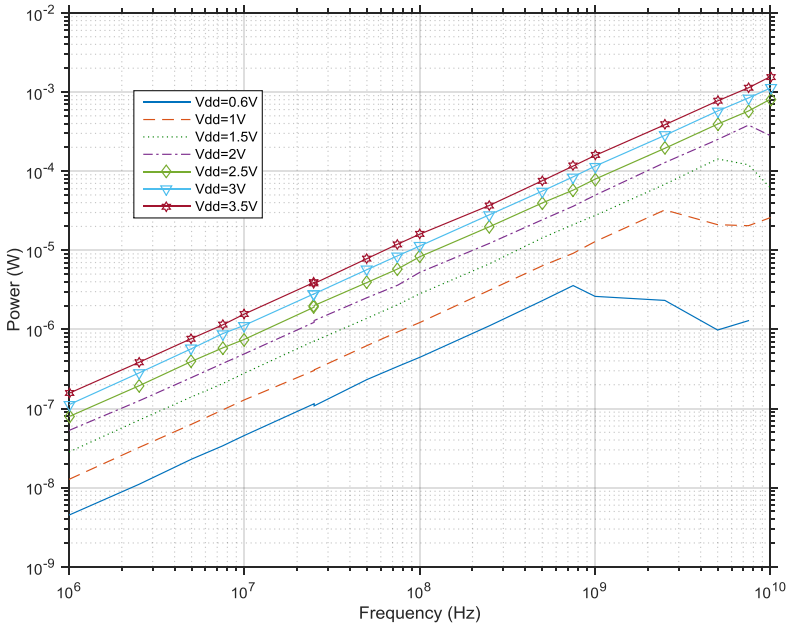


Figure (3.34): Dynamic Power Dissipation Vs Frequency of 90nm 1-Bit FA Using the Power Model.

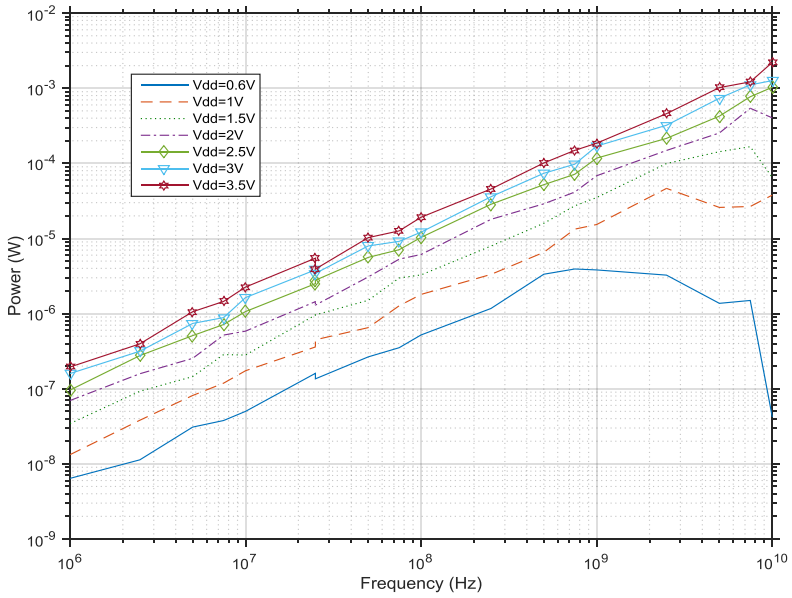


Figure (3.35): Dynamic Power Dissipation Vs Frequency of 90nm 1-Bit FA Using the OrCAD Cadence.

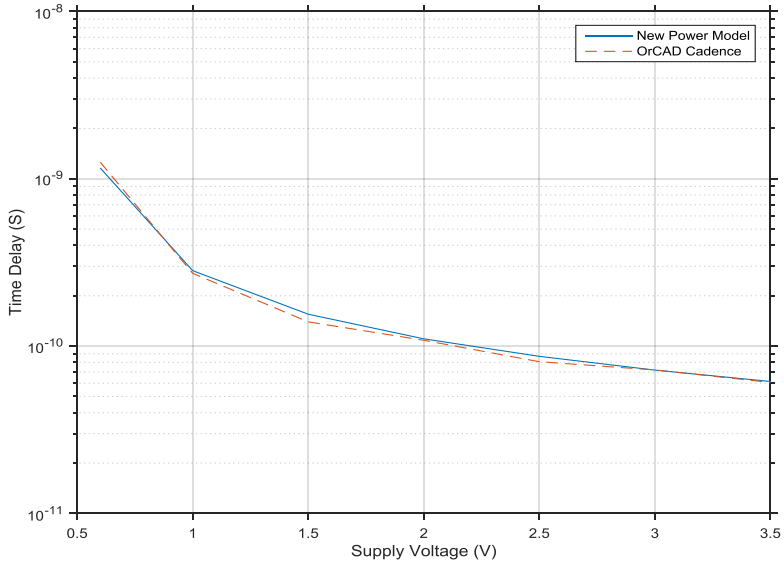


Figure (3.36): Time Delay of 90nm 1-Bit FA Using the Power Model and OrCAD Cadence.

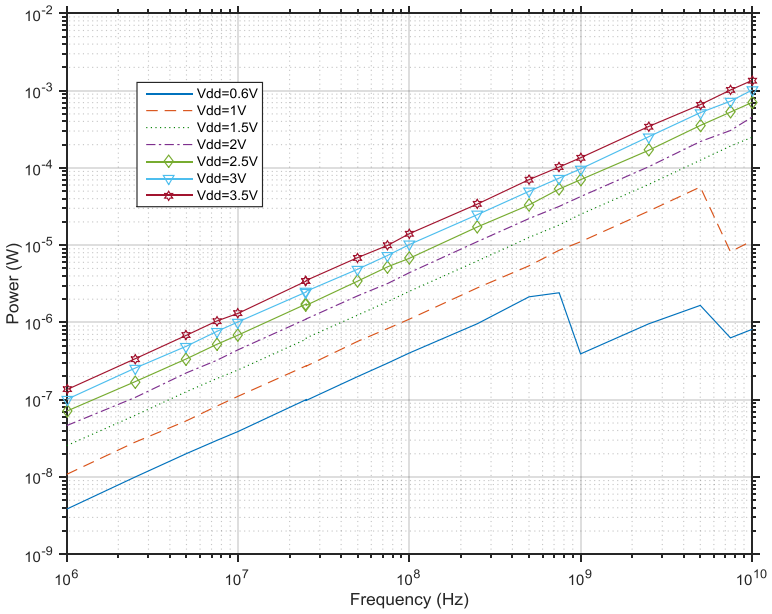


Figure (3.37): Dynamic Power Dissipation Vs Frequency of 45nm 1-Bit FA Using the Power Model.

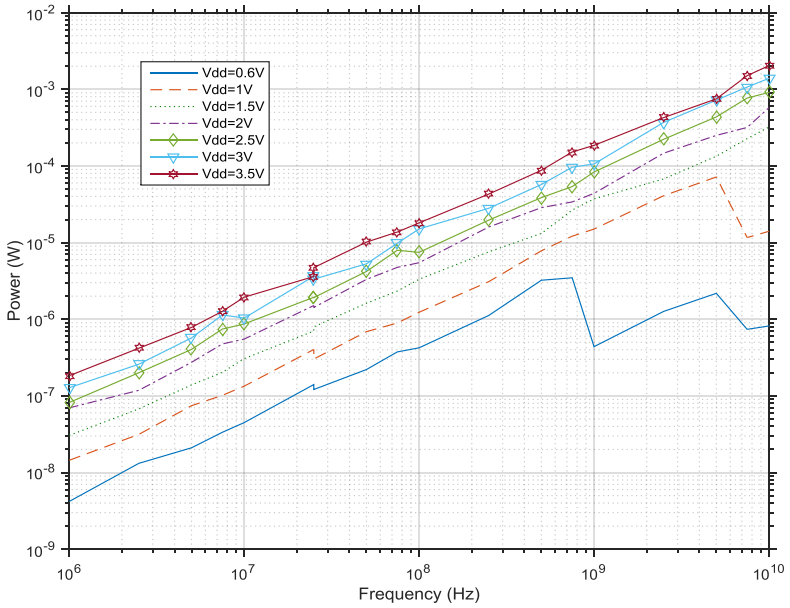


Figure (3.38): Dynamic Power Dissipation Vs Frequency of 45nm 1-Bit FA Using the OrCAD Cadence.

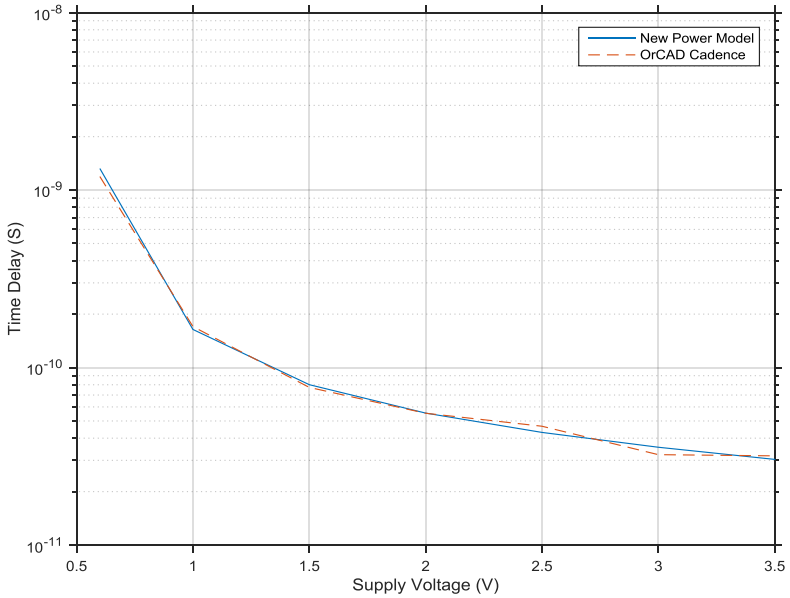


Figure (3.39): Time Delay of 45nm 1-Bit FA Using the Power Model and OrCAD Cadence.

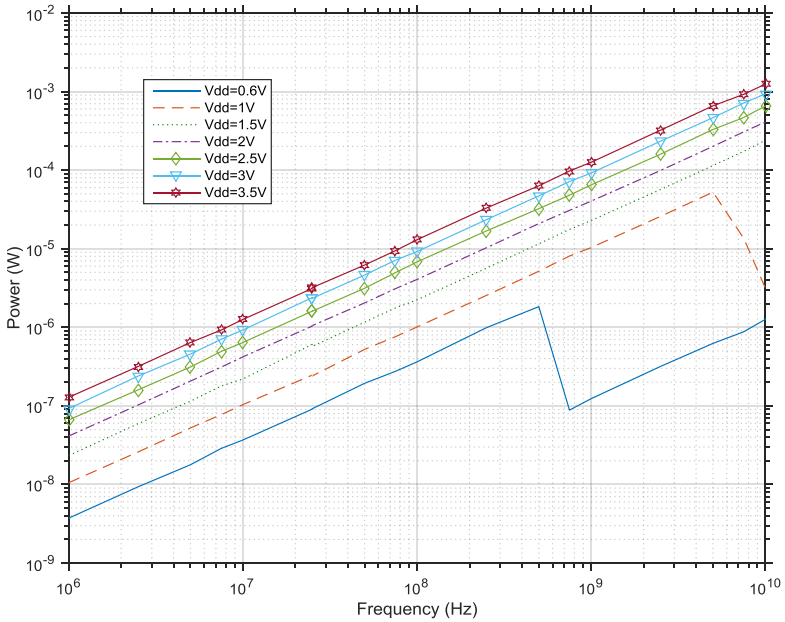


Figure (3.40): Dynamic Power Dissipation Vs Frequency of 22nm 1-Bit FA Using the Power Model.

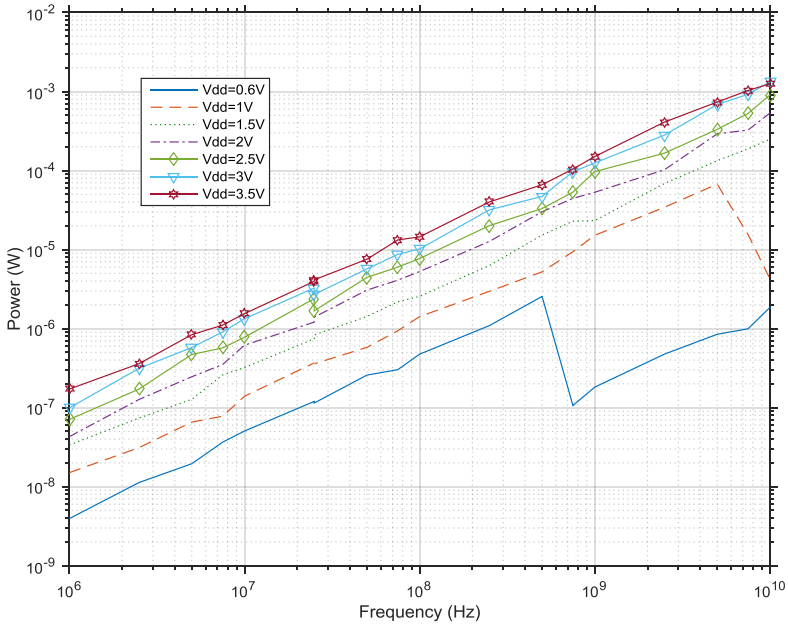


Figure (3.41): Dynamic Power Dissipation Vs Frequency of 22nm 1-Bit FA Using the OrCAD Cadence.

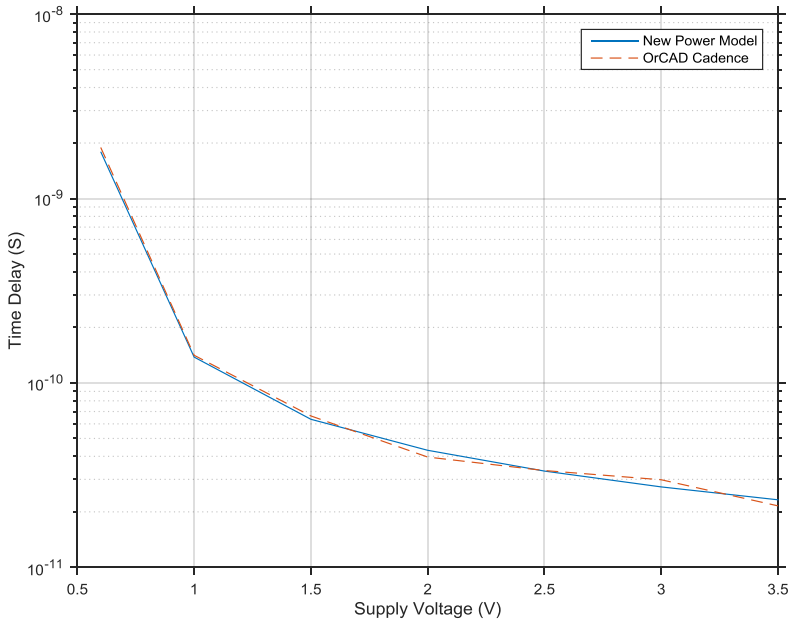


Figure (3.42): Time Delay of 22nm 1-Bit FA Using the Power Model and OrCAD Cadence.

3.4.5. Two Bit Full Adder.

The two-bit FA circuit shown in Figure (3.43) is a two cascaded one-bit FA's. It can add together two numbers, each of two bits, i.e. a_1a_0 and b_1b_0. It was chosen as a test circuit to demonstrate the ability of the new power model to work with different numbers of inputs (in this case 5 inputs).

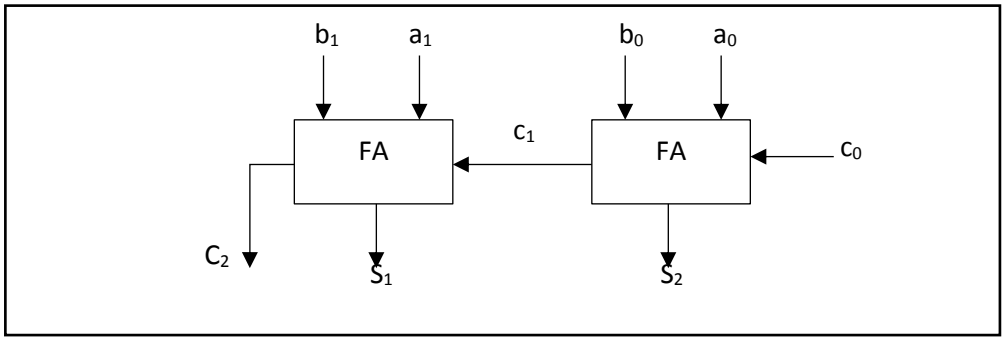


Figure (3.43): Two-Bit FA Logic Circuit.

Again, the results of the 180nm two-bit FA circuit are shown in Figures (3.44), (3.45), and (3.46), while the 90nm two-bit FA results are shown in Figures (3.47), (3.48), and (3.49). Figures (3.50), (3.51), and (3.52) present the results of the 45nm implementation of the two-bit FA, and finally, Figures (3.53), (3.54), and (3.55) show the power results and time delay of the 22nm two-bit FA circuit.

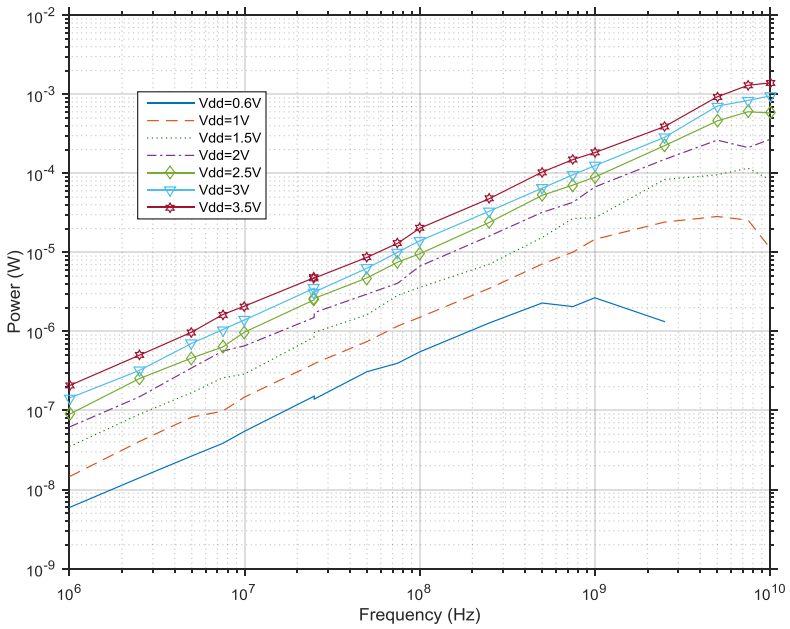


Figure (3.44): Dynamic Power Dissipation Vs Frequency of 180nm 2-Bit FA Using the Power Model.

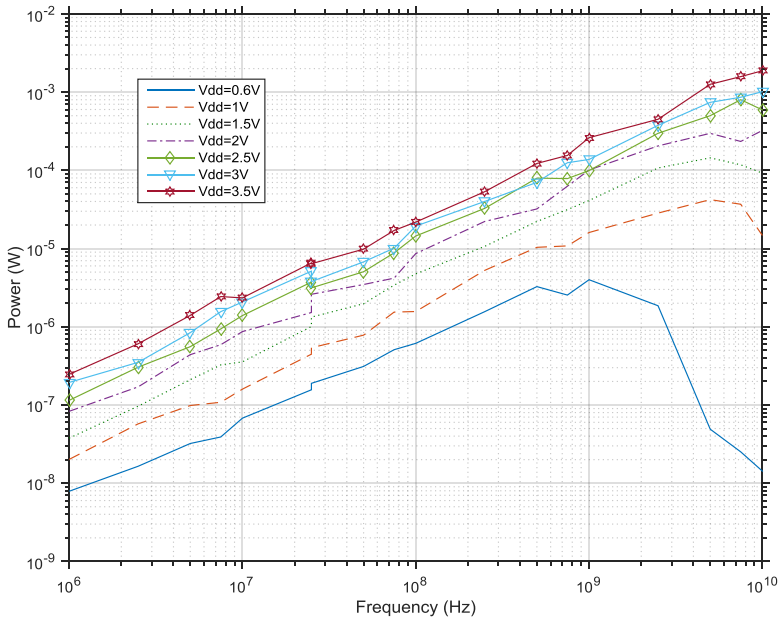


Figure (3.45): Dynamic Power Dissipation Vs Frequency of 180nm 2-Bit FA Using the OrCAD Cadence.

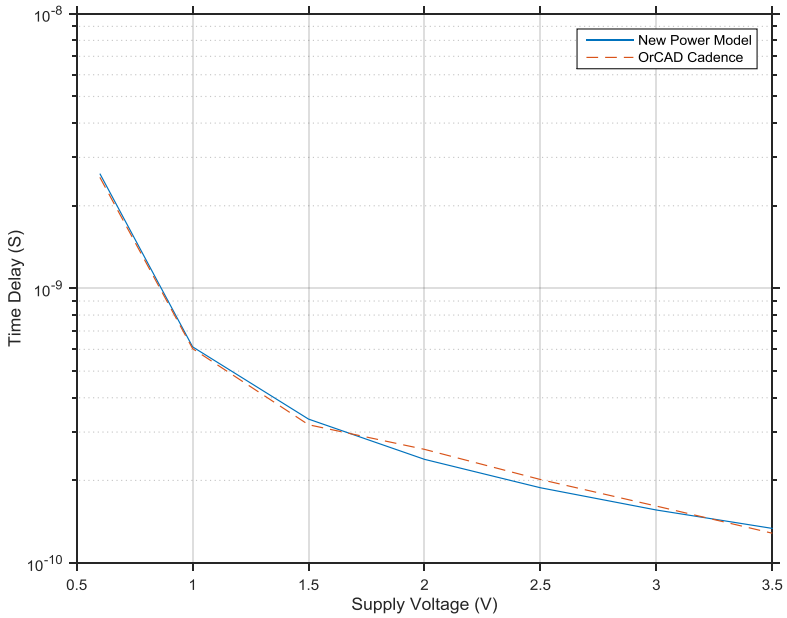


Figure (3.46): Time Delay of 180nm 2-Bit FA Using the Power Model and OrCAD Cadence.

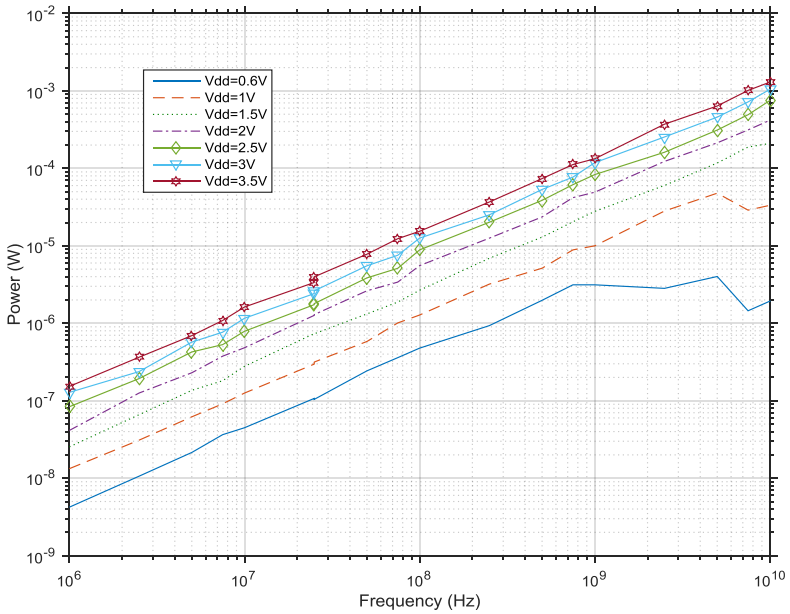


Figure (3.47): Dynamic Power Dissipation Vs Frequency of 90nm 2-Bit FA Using the Power Model.

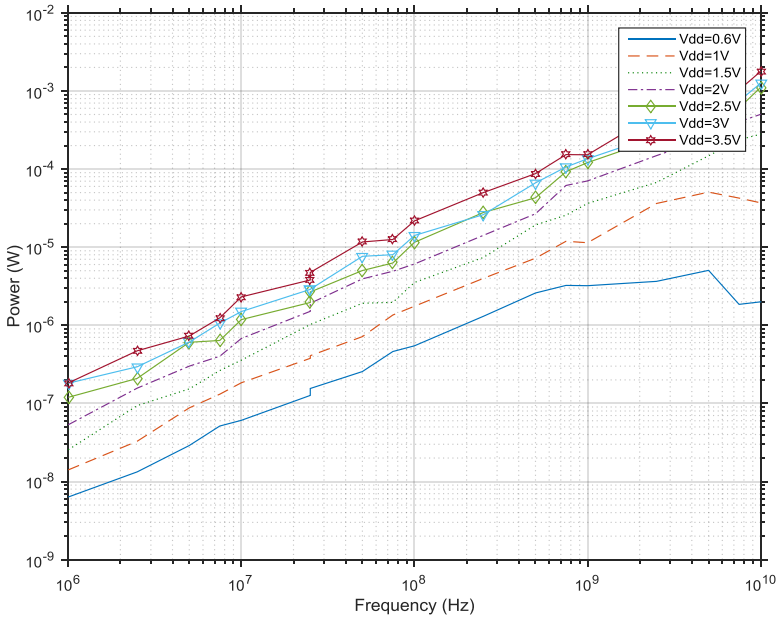


Figure (3.48): Dynamic Power Dissipation Vs Frequency of 90nm 2-Bit FA Using the OrCAD Cadence.

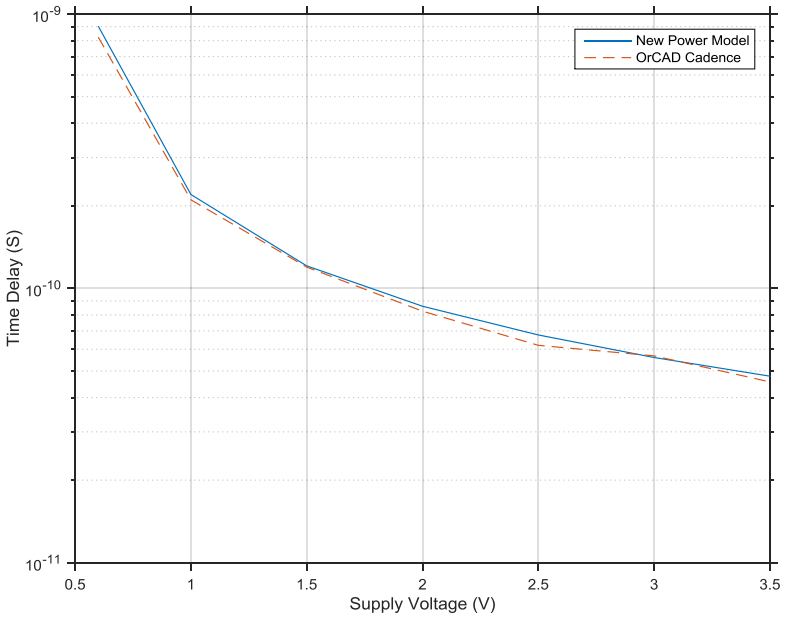


Figure (3.49): Time Delay of 90nm 2-Bit FA Using the Power Model and OrCAD Cadence.

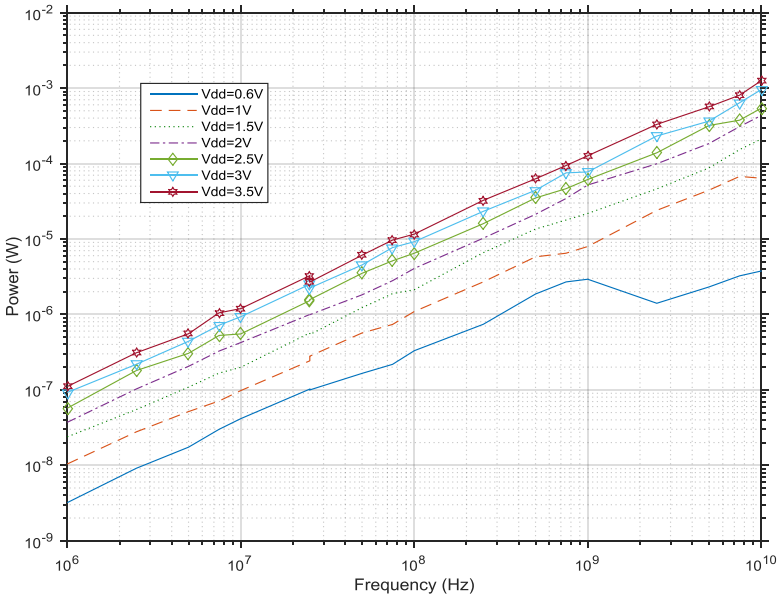


Figure (3.50): Dynamic Power Dissipation Vs Frequency of 45nm 2-Bit FA Using the Power Model.

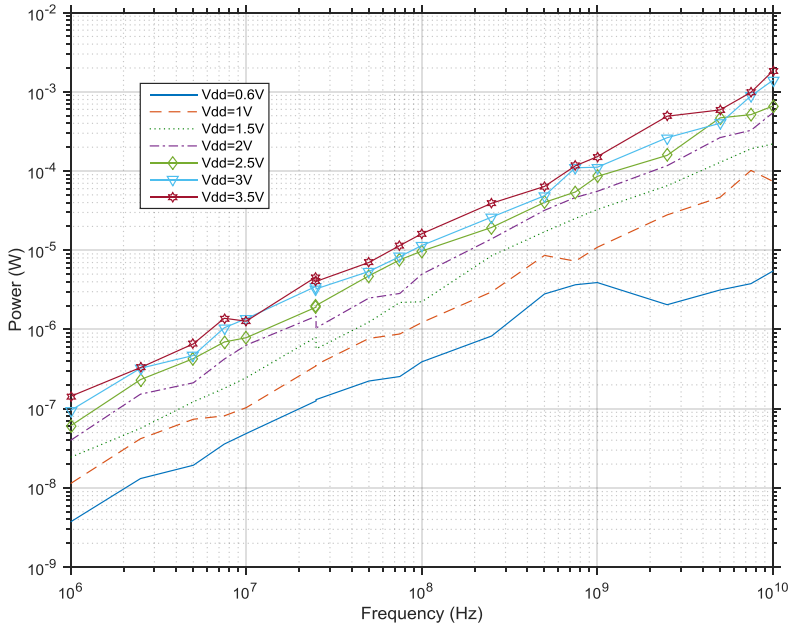


Figure (3.51): Dynamic Power Dissipation Vs Frequency of 45nm 2-Bit FA Using the OrCAD Cadence.

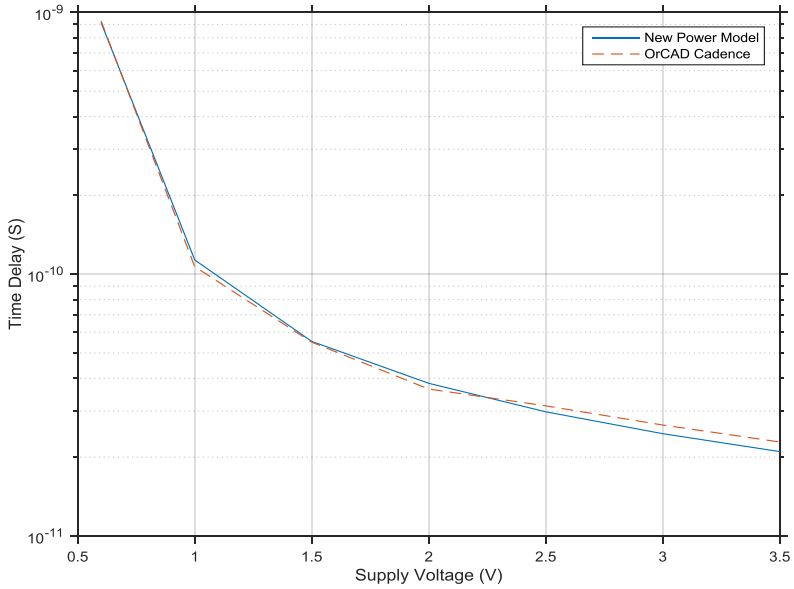


Figure (3.52): Time Delay of 45nm 2-Bit FA Using the Power Model and OrCAD Cadence.

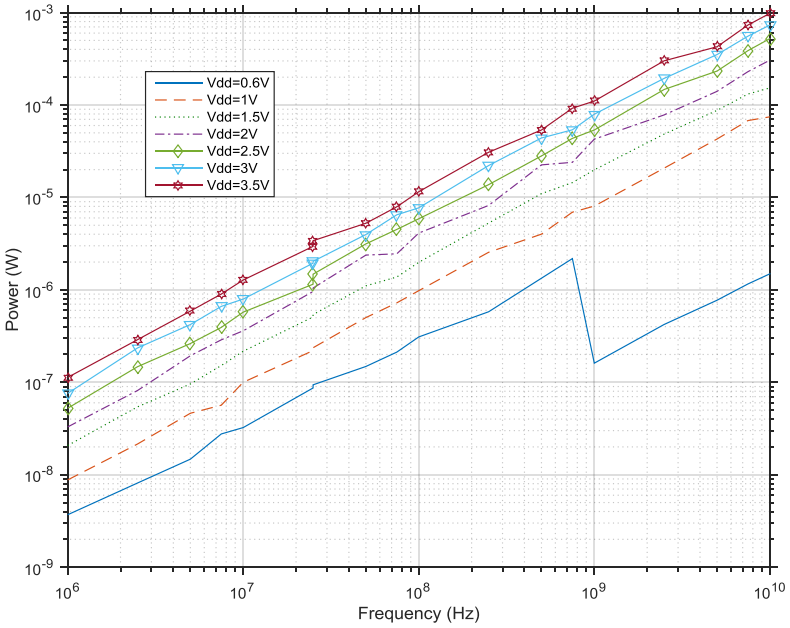


Figure (3.53): Dynamic Power Dissipation Vs Frequency of 22nm 2-Bit FA Using the Power Model.

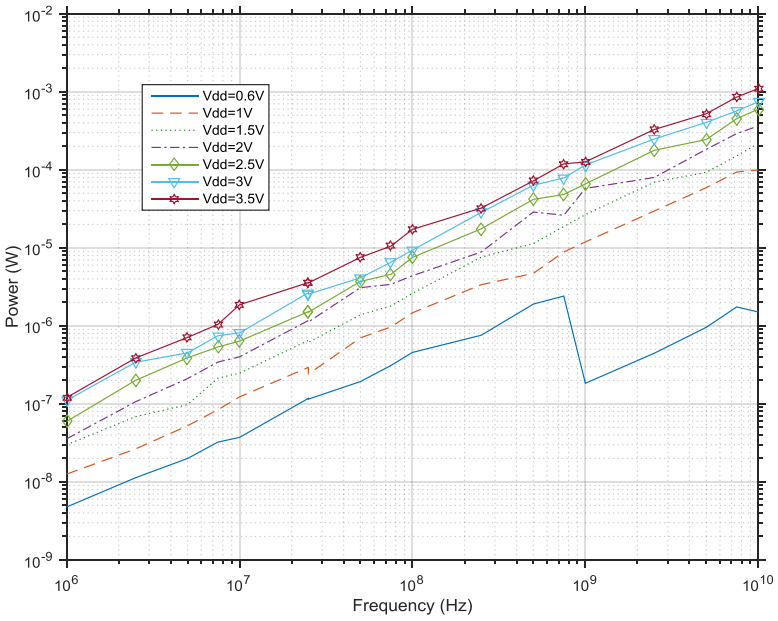


Figure (3.54): Dynamic Power Dissipation Vs Frequency of 22nm 2-Bit FA Using the OrCAD Cadence.

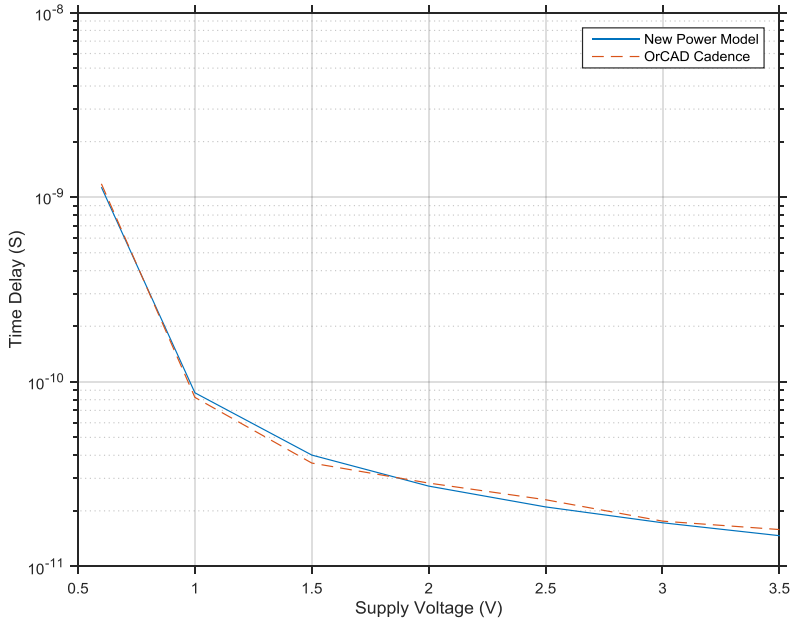


Figure (3.55): Time Delay of 22nm 2-Bit FA Using the Power Model and OrCAD Cadence.

It is common sense that the power of a 2-bit FA should be twice the power of a 1-bit FA, but that is not the case. As is obvious from comparing Figure (3.31) with Figure (3.44) at V_{dd}=0.6V, the operation range of the 1-bit FA starts from 4nW to 1.5µW while for the 2-bit FA the range is 6nW to 1.5µW. These ranges show without a doubt that although the 2-bit FA circuit is a two cascaded 1-bit FA's, the power behaviour depends on the architecture and not the number of gates. Other figures in this simulation demonstrate the same points that were discussed in sections 3.4.3 and 3.4.4.

3.4.6. Glitch Analysis

To demonstrate the effect of glitches, a simulation was carried out while omitting the effect of the time delay in the traversing algorithm of section (3.3.2). The simulation was done on a 45 nm 2-bit full adder circuit with a frequency of 100 MHz and a voltage range of 0.5 to 3.5. The aim was to demonstrate the effect of voltage change on the glitches, and hence the effect of the time delay. The results of the simulation are shown in figures (3.56).

Figure (3.56) shows that the circuit power increases as the V_{dd} increases and that the glitch power is not affected by this increase in voltage. In fact, it was measured as 10% of the consumed power for this circuit whatever the used supply voltage is. This fact is recognized if one notices that the time delay of all the gates will be affected equally with the change of V_{dd}. The only way to reduce this effect is to redesign the transistors width and length so that they

can compensate for the time delay differences in the circuit (Chou & Hung, 2015; Huda & Anderson, 2016)

This simulation was done to prove the ability of the new power model to analyse the behaviour of the glitches and their effect on the circuit power. This feature makes the new power model superior over the old power model.

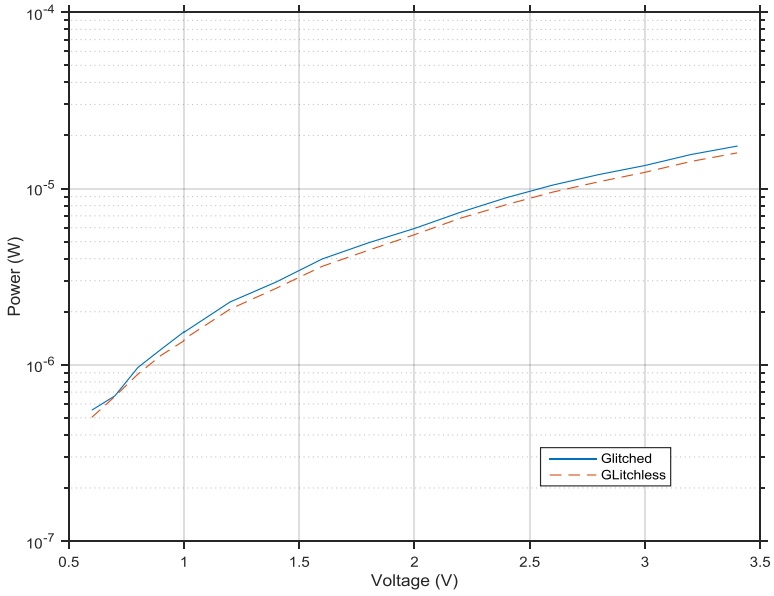


Figure (3.56). Effect of Glitches on a Two Bit Full Adder in Different Voltages.

3.5. SUMMARY AND CONCLUSIONS.

In this chapter, a second look at the existing power model was taken to determine what other parameters that affect dynamic power consumption are missing from the old power model. It was found that the old model used a constant (α) to combine the timing behaviour and the architecture of the digital circuit. A new model was built to include these new parameters in the model. Then, an algorithm was proposed to calculate the dynamic power of the digital circuit. The algorithm was implemented using MATALB and tested using different digital circuits under different conditions and with different technology sizes. Another simulation was carried out using OrCAD Cadence for the same digital circuits and under the same conditions and technology sizes. A comparison between the two simulation results showed that the new power calculation model could predict accurately the power and time delay of the digital circuits. Besides, the new model could show the frequency limits of the digital circuit, so that the

designer could decide when to increase the voltage to overcome the errors in the circuit outputs and when to reduce the voltage to gain more reduction in the dynamic power.

In the next chapter, the SPM circuit will be presented, making use of the findings in this chapter to build a power reduction algorithm. This circuit will be used in the next chapters to reduce power in different digital circuits and especially in digital communication systems.

CHAPTER FOUR

SMART POWER MANAGER UNIT DESIGN

4.1. INTRODUCTION.

There are many techniques used to reduce power in digital systems. These techniques were discussed in chapter two and it was decided that this research should use the DVFS technique as its method to reduce power. However, this technique needs a controlling entity to decide when to use it in digital circuits. Take for example ARM processors which use Intelligent Energy Manager (IEM) to control the voltage of the processor (Arm, 2007, 2008; Flautner, Flynn, & Rives, 2003). So, there is a need for a specially designed unit to control the use of DVFS technique according to the needs of the digital circuit.

In the previous chapter, the digital circuit power model was derived from the energy equation of the logic gate. In this chapter, the information acquired from the new power model are used to build SPM so that it can decide the required voltage of the digital circuit according to the used frequency and the consumed power. The SPM unit is tested using the MUX, and the 2-bit FA circuits to show its ability to reduce power in digital circuits so that it may be used in digital communication circuits.

4.2. THE NEED FOR SPM.

Using a special unit to control power dissipation in digital circuits is not a new idea. (Flynn & Rives, 2003) used their IEM to apply DVFS according to the task timing and needs. To do so, a mechanism that determines the task time must be introduced. In most research the task time allocation is the responsibility of the operating systems (Ishihara & Yasuura, 1998; Mishra & Tripathi, 2014; Williams & Constandinou, 2013). Other researchers used the measured current that supply the chip, to control the power (H. R. Pourshaghaghi & de Gyvez, 2010; Tapou & Al-raweshidy, 2012). All these researchers used an entity to control the digital circuit power through the voltage.

The control methods in these researches are not random but depend on the current status of the circuit and / or the new requirements from an external entity. E.g. (Flynn & Rives, 2003) IEM uses the information supplied by the operating system to reschedule the core voltages. (H. R. Pourshaghaghi & de Gyvez, 2010) uses the processor current to decide the new supply voltage. From the above discussion, one can conclude that there must be a smart method to determine the digital circuits need for lower power.

In digital communication systems, task time does not exist. Thus, Flynn IEM cannot be used. On the other hand, reducing the voltage according to the measured current can influence the time delay of the digital circuit and produce errors, especially when working with high frequencies. A solution to this problem is to use the frequency itself as a controlling signal

and reduce power according to it. This solution can match the needs of a multi standard communication system like (Tang et al., 2012, 2013b). Another area that can make use of such a solution is the Software Defined Radio (SDR) in which the digital communication circuits are required to work in different and high frequencies (Grayver, 2013; Iancu et al., 2015; Peng, 2010).

4.3. THE DESIGN REQUIREMENTS.

There are three main requirements needed to design the SPM unit, namely: the type of input signals, what kind of output the unit produces, and the type of controller used inside the SPM.

Since SPM is used to control the power of the digital circuits, it has to have knowledge of previous power consumption in these circuits. Hence, one of the SPM inputs is the measured power of the system. This power signal is considered a feedback that tells the SPM whether the required reduction was achieved or not.

The environment that will host SPM is the multi standard digital communication system in which the change in the standard will change the used system clock frequency. If the frequency increases, then the power will increase as well, as was shown in section (3.4). The task of the SPM is to detect this frequency change and to choose an appropriate voltage to accomplish the required power reduction. Due to that, it is wise to either supply the frequency as an input to the SPM or give the SPM unit the knowledge about the used communication standard so that it can generate the required frequency to the communication system stages.

When the voltage of the digital system is reduced, the circuit time delay is increased. Since SPM will control the power of the digital circuit through voltages, there might be a case when the voltage supplied by the SPM increases the time delay to such an extent that the circuit cannot withstand the supplied voltage. If this happens, the SPM should increase the supplied voltage, which will decrease the time delay of the system. A signal that contains the current time delay of the circuit will let the SPM unit decide the best voltage for the Communication circuit.

An elementary configuration of the SPM unit inside the communication system is shown in Figure (4.1) where the system requirement is a signal that tells the SPM unit to generate the required stage clock frequency according to the used communication standard. The digital communication system shown in the Figure is designed using (Tang et al., 2012, 2013b)

model. Each unit inside the digital communication system is responsible for a certain communication task such as Cyclic Redundancy Check (CRC), Turbo encoding, etc.

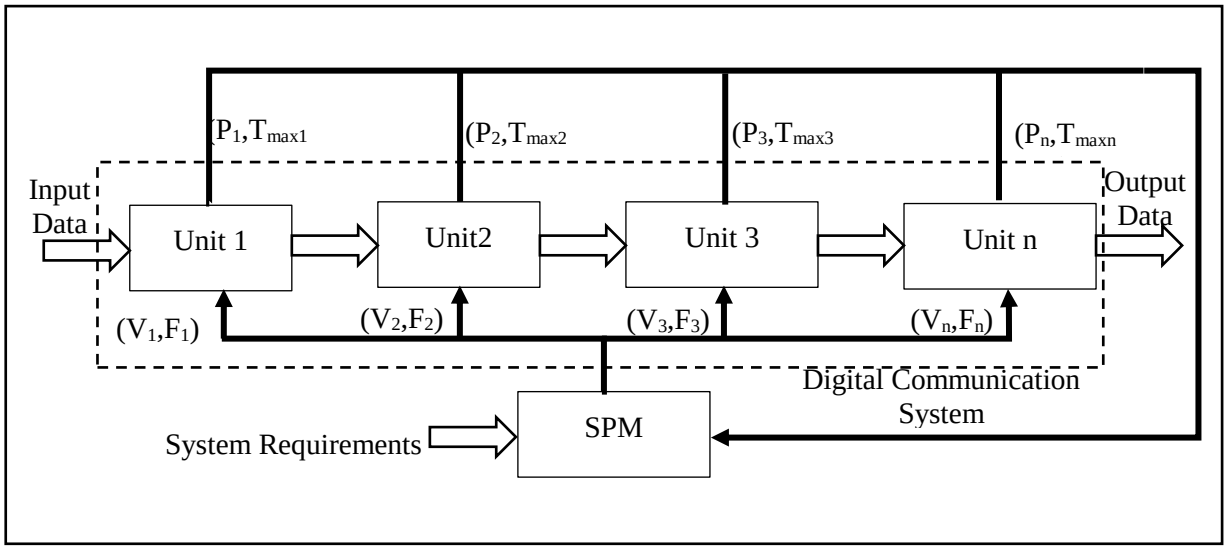


Figure (4.1): Digital Communication System with SPM Unit.

There are many types of controllers in control theory. Most of these controllers need a precise modelling for the system to be controlled so that an accurate controller is built based on the system model (Leonid, 1997). Looking at the digital system power model, it is obvious that it depends on random variables such as the architecture of the logic circuit and the number of inputs. Therefore, it is not possible to build a general classical controller for this system. Instead, the controller must look at the system model as a black box. Intelligent controllers like Fuzzy Logic Controllers (FLC) and Neural Network Controllers (NNC) are used in such systems (Lee, Vukovich, & Sasiadek, n.d.; Leonid, 1997; Murphy, 1992). NNC uses a lot of computation power and storage space, so it is not a good choice for power control. On the other hand, once the FLC is designed, it can be stored in a small ROM and used in the system. It consumes a small amount of energy and storage space (Tapou & Al-raweshidy, 2012; Tapou et al., 2011). Because of the previous discussion, SPM uses FLC to control the power in digital communication systems.

4.3.1. The Need for Coarse Control.

When V_{dd} is reduced, the circuit time delay will increase. In high frequencies, this can lead to a miss pulse error in which the circuit will not be able to produce the correct output. The missed pulse occurs because the output gates will receive their inputs late and will not have the chance to produce the correct output due to their internal time delay. This effect is clearly shown

in Figures (3.16), (3.19), (3.22), and (3.25) when the 2×1 MUX was tested under low voltage and very high frequency. This effect is reduced in two ways; either reducing the technology size or increasing the voltage and hence the power. The first solution is not applicable once the circuit is implemented which makes the second solution the best choice for such a problem.

If a miss pulse occurs, then the whole data are corrupted and that is a waste in power. So, the SPM should change its policy from reducing power consumption through reducing voltage, into reducing power consumption through saving data. This can only happen by increasing V_{dd}. A course controller was used to implement this task. The controller is simple; it works under this algorithm

1. Measure T_{max}.
2. If $F \geq {}^{1}/_{T_{max}}$ then set V_{dd} to the maximum value.
3. If $F < {}^{1}/_{T_{max}}$ then use FLC to determine V_{dd}.

So if the input frequency is 10 MHz and the calculated T_{max} corresponding to V_{dd} produced by the FLC, is 16 ns, then the F is less than $1/T_{max}$ or 10 MHz is less than 62.5 MHz. and the used supply voltage is calculated using FLC. If the frequency is 200 MHz and T_{max} corresponding to V_{dd} is 16 ns, then the course controller should use the maximum voltage as a supply voltage because 200 MHz is larger than 62.5 MHz. Such condition will ensure that the circuit time delay will not conflict with the used input frequency.

4.4. METHOD OF DESIGN.

Since the introduction of the Fuzzy sets theory by L. Zadeh back in the sixties of the last century, fuzzy logic received a good deal of attention in the field of control due to its ease of use, simplicity, robustness, and especially because it does not need the dynamics of the controlled plant since it look at the input output behaviour of the system, in another word, FLC looks at the system as a black box. Thus, it became a good choice in the controller design area (Leonid, 1997; Murphy, 1992).

For the purpose of controlling the V_{dd} value, the Mamdani type of FLC is used (Leonid, 1997), with two inputs, namely Frequency and the power, and one output, which is V_{dd}. Five linguistic sets were used to describe the fuzzy inputs, as is seen in table (4.1), which gives the sets and the range of the fuzzy inputs and output.

Table 4.1: Fuzzy Sets Specifications.

Fuzzy Set Name	Type	Fuzzy Sets					Range
Frequency	Input	Zero (Z)	Low (L)	Medium (M)	High (H)	Very High (VH)	[5 10]
Power	Input	Zero (Z)	Low (L)	Medium (M)	High (H)	Very High (VH)	[-8 -2]
V_{dd}	Output	Zero (Z)	Low (L)	Medium (M)	High (H)	Very High (VH)	[0.2 4]

In addition, the used membership function is the Gaussian distribution function given by

$$\mu(x) = e^{-\frac{(m-x)^2}{2.\sigma^2}} \quad (4.1)$$

Where m is the centre of the membership function (mean), σ is the width of the membership function (standard deviation) and x is the input variable.

The membership functions where distributed equally on the universe of discourse with the ranges shown in table (4.1). The distribution of the membership functions for the inputs and the output are shown in Figure (4.2)

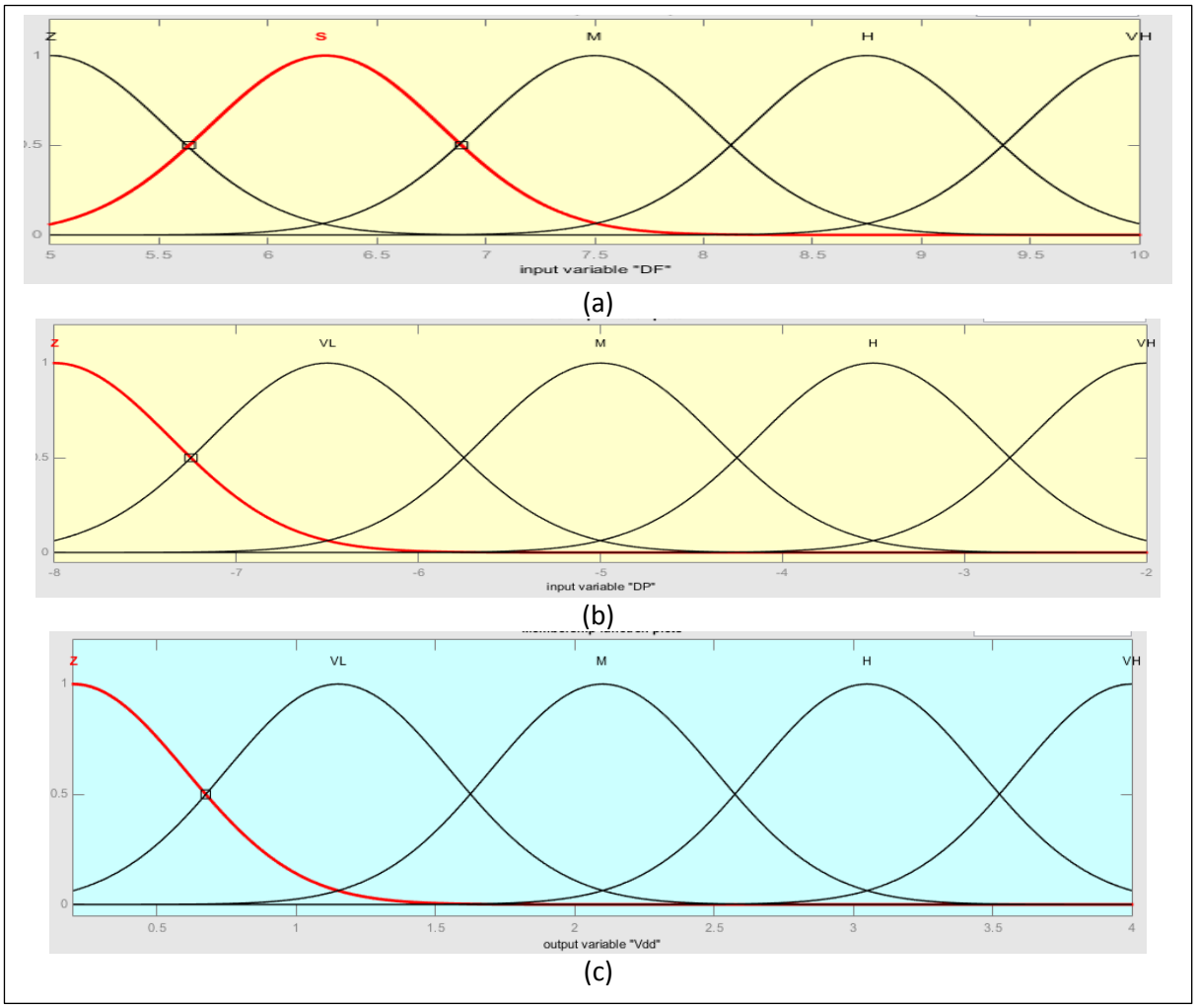


Figure (4.2): Fuzzy Membership Distribution along the Universe of Discourse, a) Frequency Memberships (input), b) Power Memberships (input), c) V_{dd} Memberships (output).

The reason behind using the Gaussian membership function is to produce a smother control surface, as it is shown in Figure (4.3). A smoother control surface will ensure a lower study state error in the system output (Leonid, 1997; Murphy, 1992).

The linguistic rules used in the FLC are shown in Table (4.2) and can be read as:

If Frequency is S and Power is VL THEN V_{dd} is Z.

Form the fuzzy rule table and by using the AND fuzzy operation, the output universe of discourse is concluded. The output of the FLC is calculated using the center of gravity algorithm.

Table (4.2): Fuzzy Rule Table.

Frequency/Power	Z	S	M	H	VH
Z	Z	VL	M	H	VH
VL	Z	Z	M	H	VH
M	Z	Z	VL	H	H
H	Z	Z	VL	M	H
VH	Z	Z	Z	M	M

The rule table and the input/ output ranges produced the control surface shown in Figure (4.3).

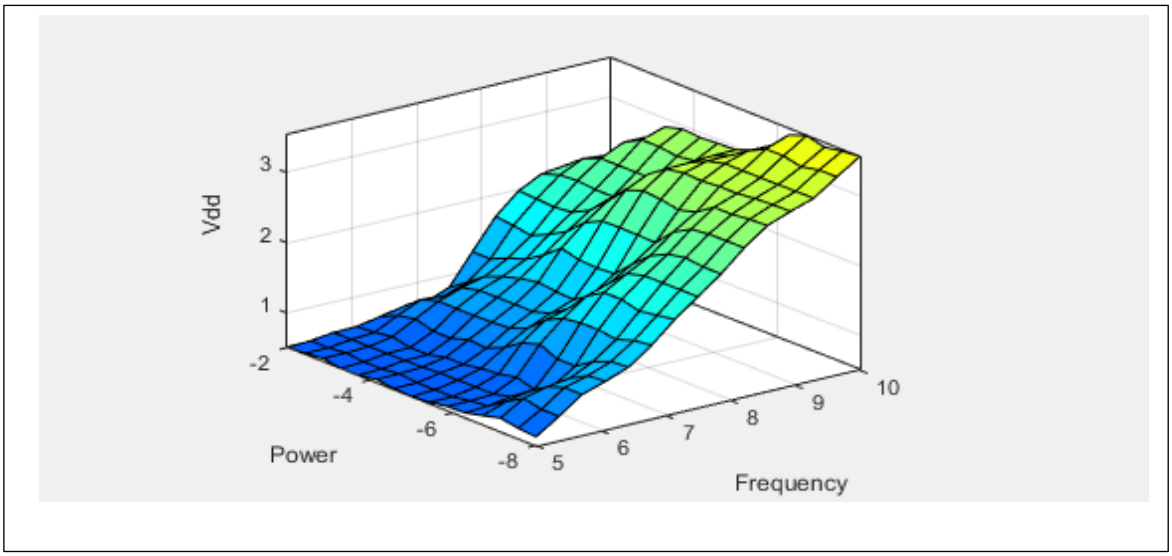


Figure (4.3): Control Surface of the proposed FLC.

In the previouse figure, it is noted that the FLC trise to reduce the voltage to its minimum value to ensure that the power consumption is at its lowest posible rate, and that is seen in the blou area of the figure. The problem arises when the frequency is high which mean

that FLC must increase the voltage so that it will overcome the missed pulse condition. This is seen in the light blue and green areas. The worst case happened when the frequency is very high, in this case FLC must produce a very high voltage to ensure a proper logic circuit operation. Since FLC does not have a knoledge about how much is the circuit T_{max}, then it has to preduct the value of V_{dd} according to the input frequency and the calculated power consumption. That explaines the ripples in the control service.

4.4.1. Choosing the Right Fuzzy Universe of Discourse.

It can be seen from table (4.1) that the ranges of the input do not represent the actual values of the expected power or frequency because the actual range of frequency will range from 1 MHz up to 10 GHz. On the other hand, the actual power may range from 10s of mW to μW, which is difficult to be fed and recognized by the fuzzy controller. Hence, a pre-scaling step was implemented to the input so that the higher and the lower ranges of both frequency and power can be recognized by the fuzzy system. The scaling of the frequency is done by taking the log of the input values, given in equations (4.2) and (4.3). This kind of scaling explains the negative values of the power range.

$$Frequency = log_{10}(F) \quad (4.2)$$

$$Power = log_{10}(P_d) \quad (4.3)$$

Throughout the literature, the input to FLC was always linear because its input was measured in a limited range. In this thesis, the range was very wide so the log scale was the choice of scaling. As far as the author knowledge this is the first time that such scaling technique is used with FLC. This scaling technique will enable FLC to contribute more in the fields where the input values has a wide range specially in high frequency communication systems.

FLC can be implemented as a ROM that contain the values of the control surface shown in Figure (4.3). The address of the bytes inside the ROM will be presented by the values of the power and frequency while the byte vale will be the V_{dd} values (Tapou & Al-raweshidy, 2012; Tapou et al., 2011). It was shown in the literature that implementing FLC in this way will add an extra 18% to the system power consumption (H. R. Pourshaghaghi & de Gyvez, 2010; Tapou et al., 2011).

4.5. IMPLEMENTATION AND RESULTS.

To test the SPM unit, two digital circuits were chosen to show the ability of the SPM to reduce their power. The circuits are the 2×1 MUX and the 2-bit FA. These circuits are the

base of every microprocessor and are found in digital communication circuits inside the modulation unit, FFT unit, and some digital encoders. It was assumed throughout this test that the circuits are working under a multi standard communication platform, i.e. the frequency is variable. Another assumption is that; since the SPM is directed to SDR hardware, it should work for low and high frequencies i.e. the frequency range should be from few MHz to GHz. The third assumption is that the frequency is generated inside the SPM and every frequency interval will last for only 1000 samples of data which should be enough to measure the power. The frequency set used in this test is shown in Figure (4.4), and its set is:

F= [3.5M 27M 130M 750M 13M 2.5G 7M 300M 650M 80M] Hz.

To equate the performance of the SPM, the system using SPM was compared to another one that has a fixed V_{dd} of 2.5V. This value is used because the circuit will be used in different frequencies, so it needed a high voltage to ensure low circuit time delay. Finally, the 22nm technology size was used in the simulation. Other technologies were omitted since the results will be redundant.

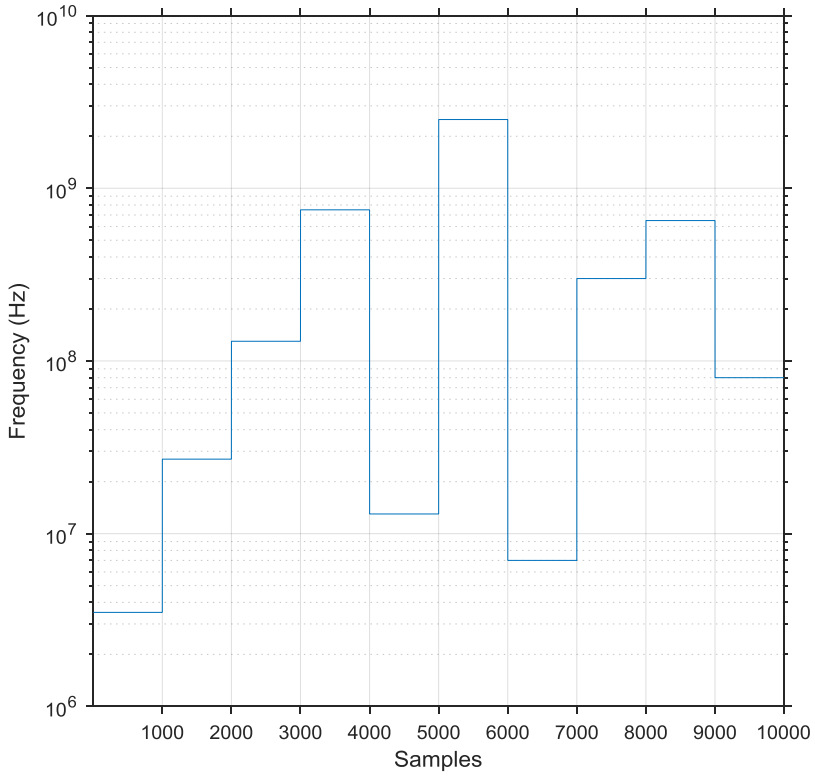


Figure (4.4): The Used Frequencies throughout the Tests of SPM.

4.5.1. The 2×1 MUX Circuit.

The 2×1 MUX circuit that was discussed in section (3.4.2) is used in this test. The results of the average power for each frequency period is shown in Figure (4.5). Figure (4.6) shows the supply voltages for each frequency period, while Figure (4.7) shows the changes in the circuit delay time. Finally, the percentage reduction in power between an ordinary system and the system with SPM is shown in Figure (4.8).

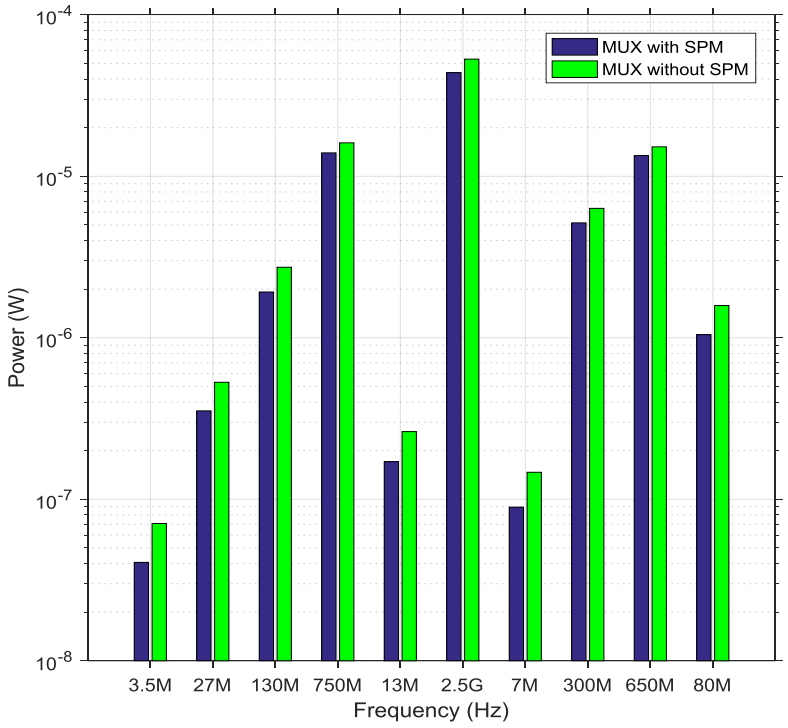


Figure (4.5): Power of the 2×1 MUX with and without SPM.

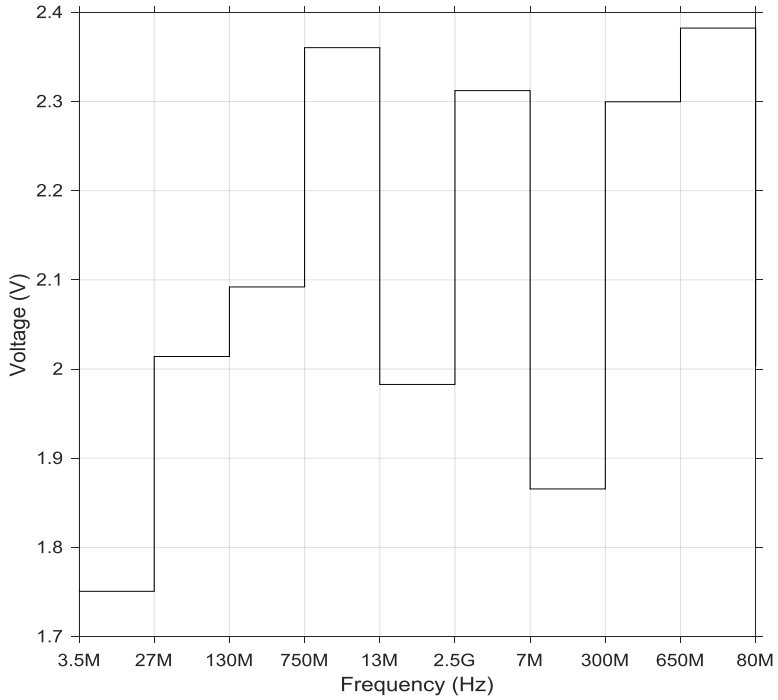


Figure (4.6): The 2×1 MUX Controlled Voltage.

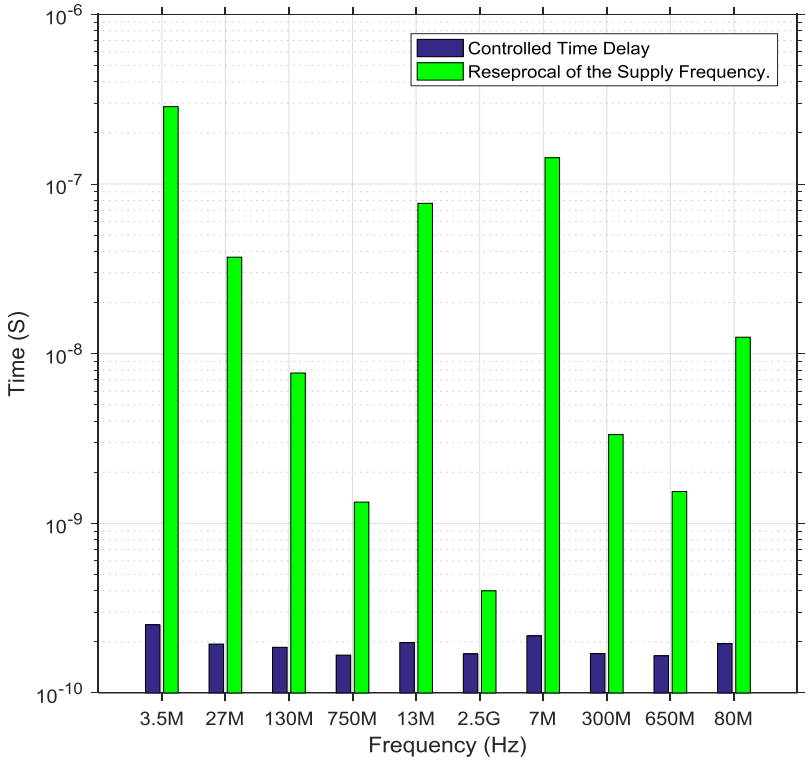


Figure (4.7): Time Delay of the Controlled 2×1 MUX.

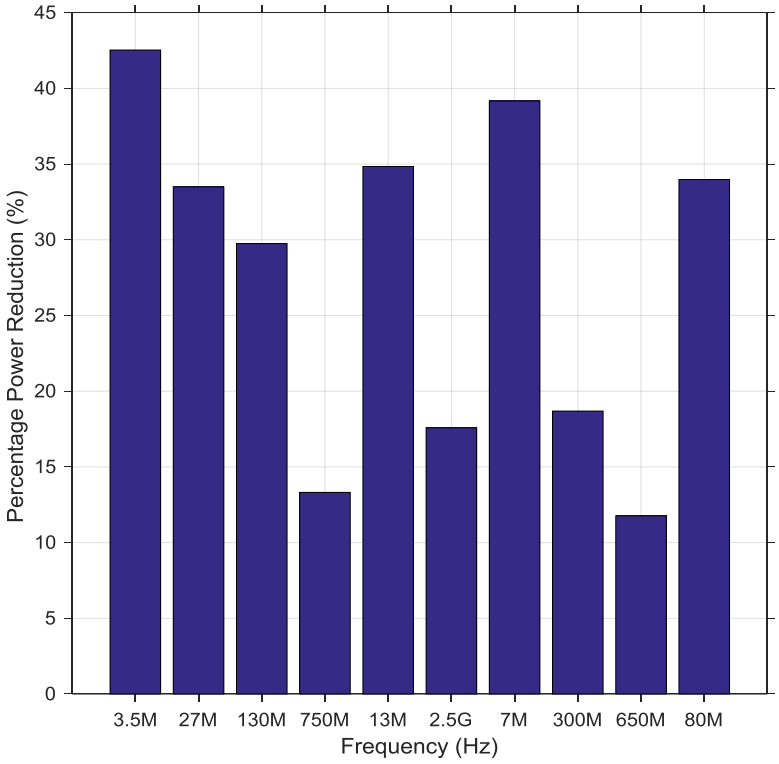


Figure (4.8): Percentage Reduction in the Controlled 2×1 MUX Power.

It is clear from Figure (4.5) that SPM is capable of reducing the consumed power of the MUX circuit considerably compared to a constant 2.5V supply voltage. The voltage in Figure (4.6) shows that even when the frequency is very high (2.5GHz), the supply voltage managed to stay low at 2.35V, which led to a good reduction in power in this frequency. It is worth noting that the voltage at 750MHz is larger than that of the 2.5GHz due to the scaling technique that was used in the FLC. This scaling technique needs to be reconsidered to obtain a better power reduction in such frequencies. The time delay of the circuit is always below the reciprocal of the supply frequency, which means that the input gets enough time to propagate through the circuit even when the frequency is very high. Finally, the percentage of power reduction of the circuit, Figure (4.8), shows that the SPM can decrease power in the range of 13- 43 % depending on the used frequency.

4.5.2. The 2-Bit FA Circuit.

The two-bit FA circuit that was discussed in section (3.4.4) is used in this test. The results of the average power for each frequency period appears in Figure (4.9). Figure (4.10) shows the supply voltages for each frequency period while Figure (4.11) shows the changes in

the circuit delay time. The percentage reduction in power between an ordinary system and the system with SPM is presented in Figure (4.12).

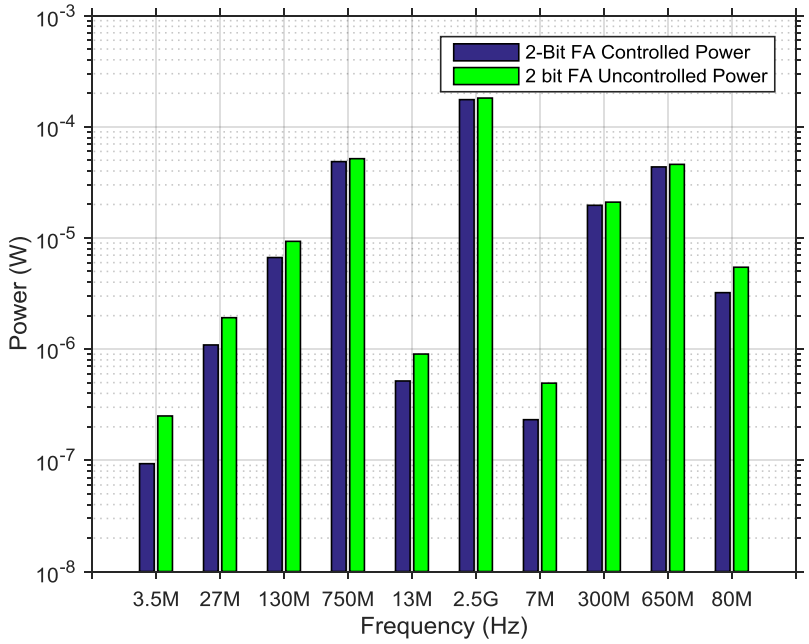


Figure (4.9): Power of the 2-Bit FA with and without SPM.

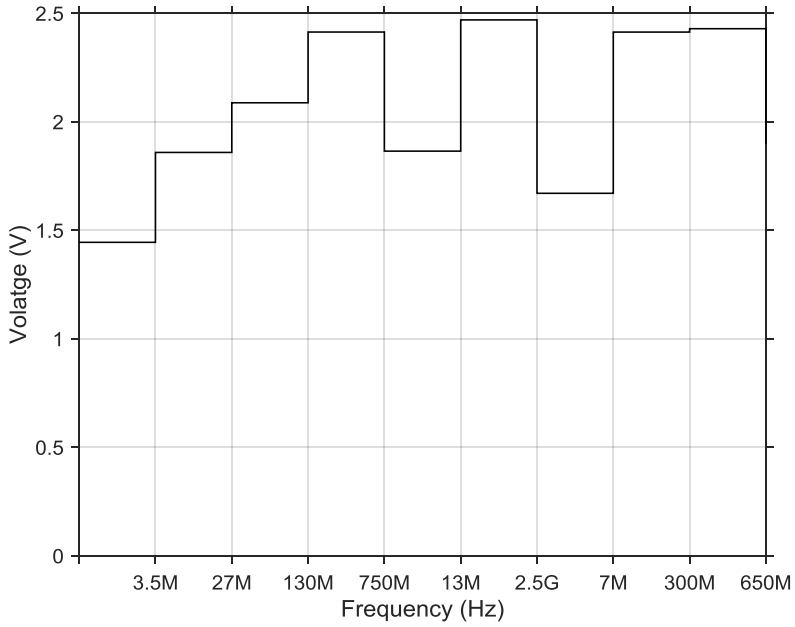


Figure (4.10): The 2-Bit FA Controlled Voltage.

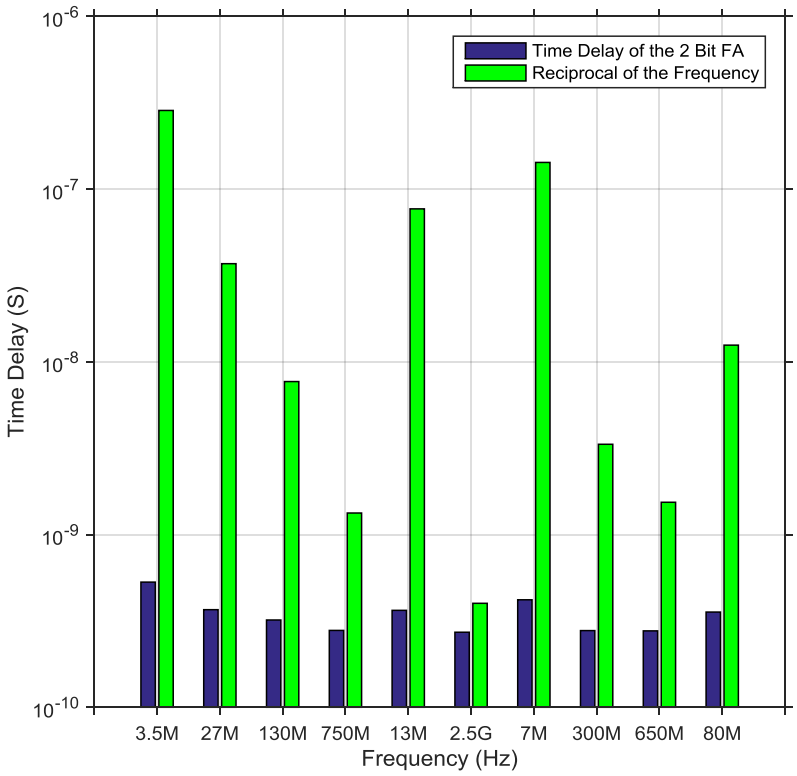


Figure (4.11): Time Delay of the Controlled 2-Bit FA.

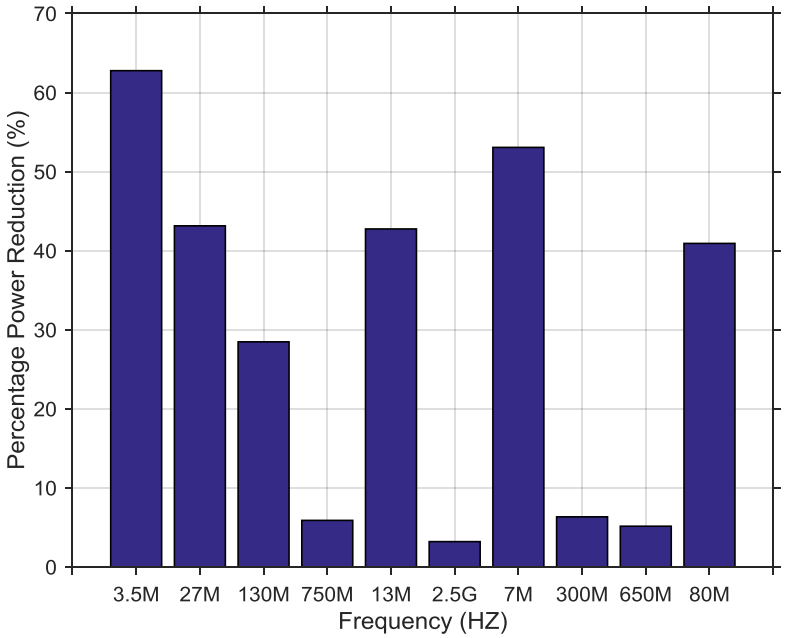


Figure (4.12): Percentage Reduction in the Controlled 2-Bit FA Power.

From the figures above, it is clear that SPM can reduce the power of the two-bit FA circuit by reducing V_{dd}. At the same time, SPM managed to keep the time delay of the circuit below the reciprocal of the supply frequency which guarantees an error free output of the circuit. In high frequency (2.5GHz), the voltage is at its highest value (2.4V) to overcome the time delay problem. The percentage of power reduction lies between 4 and 63 %. It is clear if the input frequency is low, more power reduction is achieved.

4.6. SUMMARY AND CONCLUSIONS

In this chapter, the design of the SPM block was discussed. Its input requirements were clarified as the system input frequency, circuit time delay and the current power consumption. FLC was chosen as the main voltage controller that ensures good power reduction. Alongside FLC, a coarse controller was used to ensure that the system does not produce error due to high time delay. The FLC universe of discourse scales were chosen so that the input is mapped to the fuzzy input set correctly, although the range between the lowest expected input and the highest one is very wide. The FLC was chosen to minimize the power consumed in the controlled circuit and, at the same time, maintain a low time delay for the circuit.

SPM was tested using two circuits; the 2×1 MUX and the two-bit FA circuits. The results showed that SPM could successfully reduce power in both circuits even when the required input frequency was changing randomly from high to low and to high again. The results also showed that SPM managed to keep the circuit output error free by maintaining a low circuit time delay even when the frequency is high. The percentage power reduction using SPM is high at low frequency and it decreases when the frequency increases. The previous discussion proves that SPM can work in digital communication environment, especially for SDR and multi-standard communication systems.

In the next chapter, one of the widely used circuits in communication systems is introduced. CRC circuit will be designed in a parallel way and modified to work for different generators. The circuit will then be used as a test circuit with the SPM to prove the ability of SPM to work with communication circuits.

CHAPTER FIVE

MULTI POLYNOMIAL CRC DESIGN FOR COMMUNICATION PURPOSES

5.1. INTRODUCTION.

When sending data through a noisy channel, errors appear in the received data. To identify these errors and correct them, channel coding is used. One of the commonly used circuits in error detection in communication systems, is the CRC circuit (Guizani, 2004; Stremler, 1990). Its simple design and versatile use in communication systems make it a good contender to measure power.

Until now, this thesis discussed the power in digital systems, built a model to measure it, and built SPM to control it. To link the previous work to communication, there is a need to apply the SPM inside a communication system. As CRC exists in almost every communication system, its power will be the target of this research. In this chapter, three types of CRC circuits are to be designed, namely: the 8, 16, and 24-bit CRC circuits. These three circuits were chosen because they are the norm of the LTE communication systems. In the final stage of this chapter, a multi polynomial method of design is introduced to produce a circuit capable of generating the CRC remainder for different generators. This circuit reduced the number of used gates, which in turn reduced the consumed power.

5.2. CRC IN COMMUNICATION SYSTEMS.

Due to the huge development in the means of communication, massive amounts of data are transferred from multiple sources to their destinations. These data need to be protected from channel noise and error. One of the widely used methods for protecting data is the CRC (Haykin, 2008). In CRC, a polynomial is chosen to generate a code that is attached to the end of the data to produce a frame. After transmitting the frame, this code is regenerated in the receiver and compared with the transmitted one to decide whether the transmitted data were correctly received or not (Sprachmann, 2001). The polynomial is given as:

$$g(x) = g_n X^n + g_{n-1} X^{n-1} + \cdots + g_1 X + g_0 \qquad (5.1)$$

g_i is the polynomial i^{th} position coefficient and X_i is the bit position. It is worth saying that the value of g_i is either 0 or 1.

The method of generating CRC digitally is based on the Linear Feedback Shift Register (LFSR), shown in figure (5.1), in which the data u(i) are fed to the register serially and XORed with the generator bits g_k in each clock cycle (M. Ayinala & Parhi, 2010). The circular × in the figure represents the AND operation and the circular + is the XOR operation. The D box is the D type flip-flop. The initial stage of the these flip-flops are all zeros.

The latter method (Sprachmann, 2001) is unfeasible in fast communication systems. Its throughput (number of processed bits per second) is very small because the remainder bits are calculated in a serial manner (one bit per cycle) (Condo, Martina, Piccinini, & Masera, 2014). Researchers focused in their work on this circuit to speed up its performance through many methods like unfolding, lookup tables, and retiming (Manohar Ayinala & Parhi, 2011; Condo et al., 2014; Derby, 2001; Grymel & Furber, 2011; Haykin, 2014; Ma & Cheng, 2011; Sprachmann, 2001)… etc.

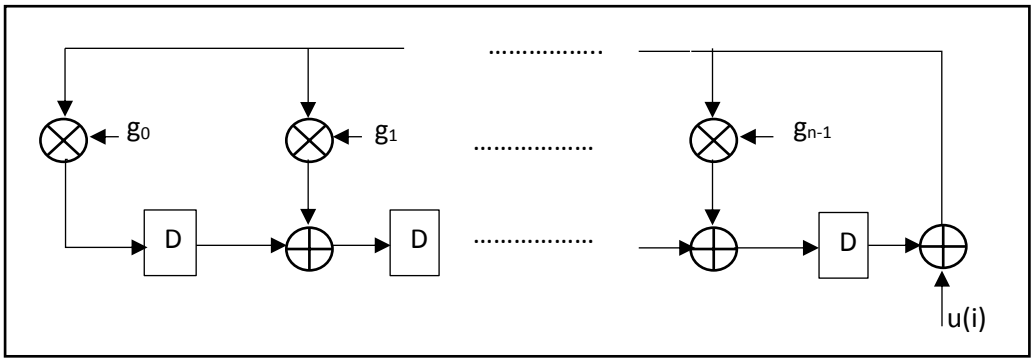


Figure (5.1): Basic Linear Feedback Shift Register (LFSR)

In 2001, Sprachmann (Sprachmann, 2001) built an adaptive parallel architecture that is capable of producing CRC bits in parallel rather than serial. The design is based on the state machine method, and it can be modified to take different CRC generators. Yet, it is not capable of handling different polynomials at the same time.

A state space approach to facilitate parallelism in CRC was introduced by Derby (Derby, 2001). This research was the base for many developers to produce their own designs and algorithms. One of the developments is to use a selector matrix to decide which XOR gate to use for updating the state registers (Grymel & Furber, 2011). The author demonstrates the capability of the design to produce many kinds of CRC circuits, but still, the circuit can only work with one polynomial at a time.

Cheng and Parhi explored the use of unfolding, pipelining, and retiming to increase the performance of the CRC circuit (Cheng & Parhi, 2006). Nevertheless, the design is directed towards one CRC polynomial and it cannot work with different CRC polynomials at the same time.

Another investigation on the critical path and the fan out of the nodes to improve the performance of the LFSR were discussed in (M. Ayinala & Parhi, 2010; Manohar Ayinala &

Parhi, 2011). CRC was used because its architecture is based upon LFSR, but the algorithm still lacks the use of multi-polynomials in one circuit.

The first to introduce a fully configured CRC circuit that can work with different types of polynomials are Toal, McLaughlin, Sezer and Yang (Toal, Mclaughlin, Sezer, & Yang, 2009). However, their work is based on a huge selection matrix that makes the circuit area large, and hence, leading to higher power consumption. The same method was developed and enhanced by slicing the polynomial into a number of small parts that are executed in a parallel fashion in (Cho, Sung, & Sung, 2010), but the large area problem was not solved in this research.

The effect of the input buffer on the calculation process of the CRC is investigated in (Grymel & Furber, 2011), to produce a higher speed CRC. The algorithm is suitable for any type of generator. Moreover, the method is enhanced and introduced to the 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) communication system in (Condo et al., 2014). The inability to deal with many polynomials still exists in these researches.

5.2.1. CRC in LTE communication systems.

Due to its well-defined mathematical structure and ease of use, CRC is widely implemented in communication systems (Haykin, 2008). LTE and LTE- Advanced (LTE-A) use CRC for channel coding. Since the data rate is not fixed in this technology, four types of CRC polynomials are used leading to the need for four different circuits for each polynomial. The used polynomials are (3GPP Specifications, 2015c):

$$g_{CRC24A} = X^{24} + X^{23} + X^{18} + X^{17} + X^{14} + X^{11} + X^{10} + X^{7} + X^{6} + X^{5} + X^{4} + X^{3} + X + 1 \quad (5.2)$$

$$g_{CRC24B} = X^{24} + X^{23} + X^{6} + X^{5} + X + 1 \quad (5.3)$$

$$g_{CRC16} = X^{16} + X^{12} + X^{5} + 1 \quad (5.4)$$

$$g_{CRC8} = X^{8} + X^{7} + X^{4} + X + 1 \quad (5.5)$$

X^i indicates the bit position in the polynomial.

LTE and LTE-A use these polynomials for their data verification process and as a stopping condition for the turbo coding stage (Cox, 2012). So, they need a circuit that can perform all of the four types of CRC mentioned above, rendering a large number of gates and a large area to implement them. This leads to higher power consumption. Fortunately, many

communication systems use g_{CRC16} as the base for their CRC stage, so an algorithm to combine three of the polynomials is introduced. This algorithm will insure a reduction in the area used for the CRC circuit leading to decreasing the power consumption in this circuit. The algorithm dealt with g_{CRC8} g_{CRC16}, and g_{CRC24B} only and neglected g_{CRC24A} due to the method of its use with g_{CRC24B} discussed below.

g_{CRC24A} is used when the transmitted frame size is bigger than the maximum frame size. The frame size is 6144 bits in LTE. If this happens, LTE will apply g_{CRC24A} to the total frame, and then separate it into two sub-frames each of 6114 bits and apply g_{CRC24B} to each of them individually. This is shown in figure (5.2) (3GPP Specifications, 2015c). The CRC method just described, implies the use of g_{CRC24A} and g_{CRC24B} together or in parallel to produce the final frames. Due to this, it is impossible to combine both polynomials in one circuit. On the other hand, g_{CRC24A} is only used when the data size is more than the maximum size, which is not the typical case. As for the g_{CRC16} and g_{CRC8}, they are used in different channels in LTE and LTE-A (3GPP Specifications, 2015a, 2015b). using different channels will make it possible to combine the CRC circuits associated with each channel in one circuit. Hence, the design will introduce an algorithm to combine only g_{CRC8}, g_{CRC16} and g_{CRC24B} into one circuit.

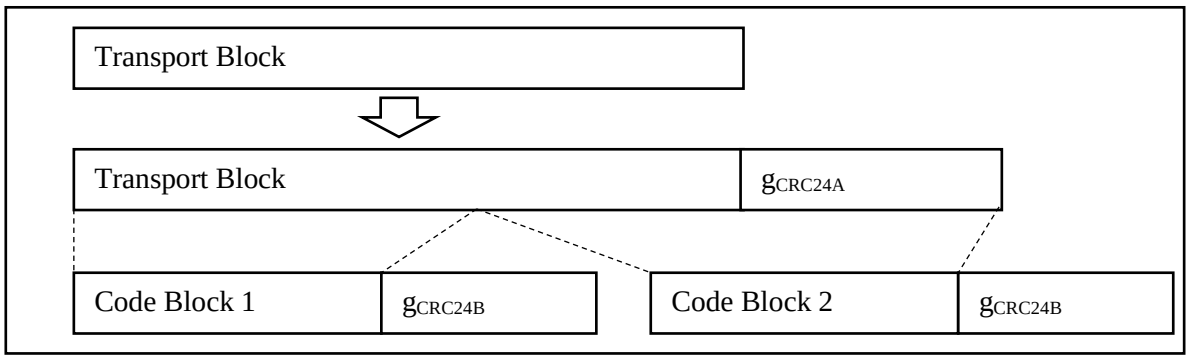


Figure (5.2): Insertion of CRC24A and CRC24B in LTE

5.3. PARALLEL CRC CIRCUIT DESIGN.

In this section, the design of parallel CRC circuit is introduced to provide the needed information for the CRC combination algorithm.

The parallel circuit is based on LFSR shown in figure (5.1). It can be looked at as a Linear Time Invariant (LTI) system. The input for the LTI is the data bits u(i), the states are the remainders x(k) that are stored in the flip flops (referred to as D, in figure(4.1)) (Manohar Ayinala & Parhi, 2011; Derby, 2001), and the output of the circuit is the remainders. The equation that governs the operation of the circuit is:

$$x(k+1) = A.x(k) + B.u(k) \quad (5.6)$$

$$y(k) = C.x(k) + D.u(k) \quad (5.7)$$

y(k) is the system output, while A, B, C and D are the state matrices. It should be noted that the operations between the matrices are the ordinary AND, represented by the dot, and the XOR, represented by the plus sign. In other words, the operations are in the Galois Field GF(2) (Campobello, Patan??, & Russo, 2003).

For the case in which y(k)=x(k), the state matrices can be written as:

$$A = \begin{bmatrix} 0 & 0 & 0 & \dots & 0 & g_0 \\ 1 & 0 & 0 & \dots & 0 & g_1 \\ 0 & 1 & 0 & \dots & 0 & g_2 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & 1 & g_{n-1} \end{bmatrix}, B = [g_0 \quad g_1 \quad \cdots \quad g_{n-1}]^T, C = I, D = 0 \quad (5.8)$$

I is the identity matrix.

By repeatedly calculating the value of X for ω times, one can get ω number of remainder bits in one operation. Additionally, by unfolding the system with the folding factor of ω, one can get the following equation (Manohar Ayinala & Parhi, 2011; Campobello et al., 2003; Derby, 2001):

$$x(k+1) = F^{\omega}.(x(k) \oplus u(k)) \quad (5.9)$$

F^{ω} is calculated from the following recursive formula:

$$F^1 = A, F^i = \left[F^{i-1} + \begin{bmatrix} g_0 \\ g_1 \\ \vdots \\ g_{n-1} \end{bmatrix} \middle| \begin{matrix} \text{the first } n-1 \\ \text{columns of } F^{i-1} \end{matrix} \right] \quad (5.10)$$

where i is an integer from 1 to ω.

Equation (5.10) represents the unfolded system and it can produce ω remainders at each clock cycle. To calculate F^{ω}, F^1 is equal to A and is calculated as in equation (5,8) then F^2 is calculated by taking the sum of F^1 and the concatenating result of the g column vector and the first to the n-1 columns of F^1. By repeating the procedure to ω times, F^{ω} is obtained.

To implement the CRC circuit using equations (5.9) and (5.10), a VHDL programme was written to represents the 8, 16, and 24-bit CRC circuits. The implementation took place on

a Terasic DE4 board based on the Altera Startix IV FPGA (Terasic, n.d., 2015). The design and implementation process for each circuit is described below:

5.3.1. 8-bit CRC circuit design.

By applying equation (5.10) into equations (5.9) and choosing ω=8, F^8 is given in hexadecimal form as:

$$F^8 = [47 \quad 64 \quad 32 \quad 19 \quad CB \quad 22 \quad 91 \quad 8F]' \tag{5.11}$$

The superscript (‘) represents the transpose of the matrix. By using equation (5.10), the circuit that represents the 8-bit CRC is shown in Figure (5.3). This circuit used 13 FPGA logic elements, and 8 dedicated registers. Using FPGA logic elements means that the FPGA chip is using its Adaptive Logic Module (ALM) to represent the logic gates. Sometime one ALM can represents more than one logic gates, which explain why the number of FPGA logic gates is less than the logic gates in the circuit of Figure (5.3).

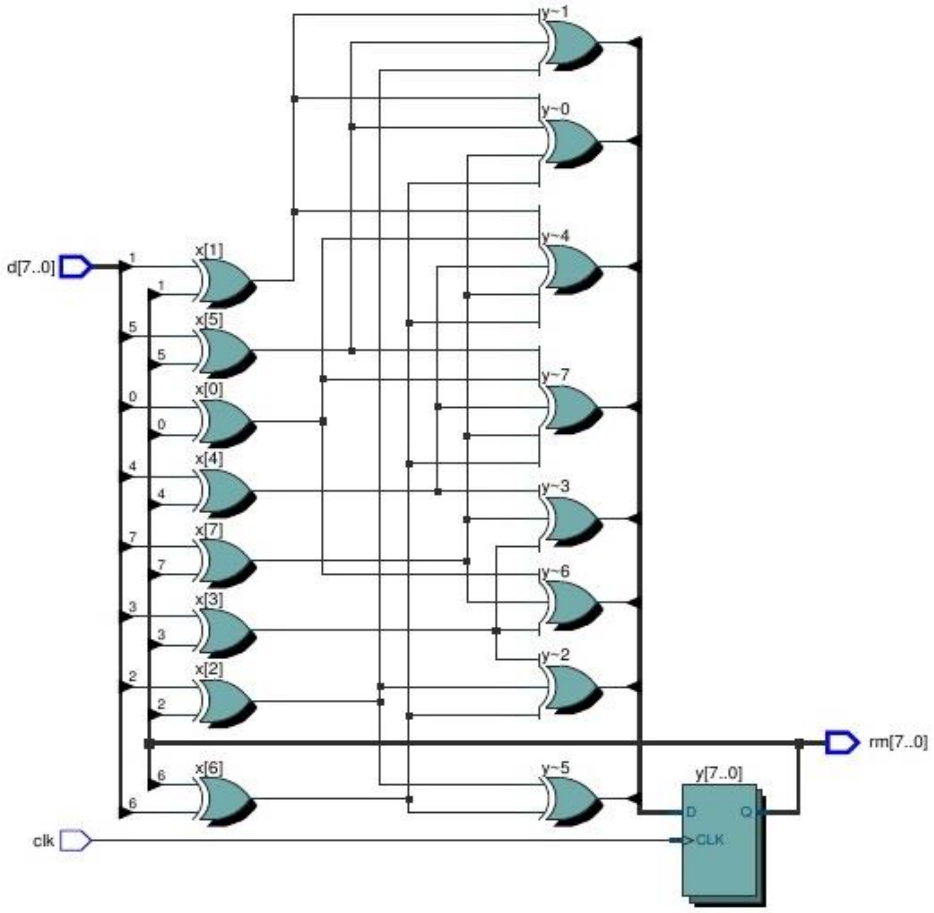


Figure (5.3): Implementation of the 8-Bit CRC Circuit.

The circuit of Figure (5.3) uses d[7..0] as its 8 bit input u(k) to the XOR tree. It take the remainder rm[7..0] as a feedback that represents the current state remainder vector X(k). When the clock signal clk is activated the current remainder state and the input are both processed to produce the next state reminder X(k+1) which is stored in the y[7…0] register. The register presents the X(k+1) remainder as rm[7…0] in the next clock cycle.

To verify the operation of the CRC8 circuit, the circuit was simulated using Altera ModelSim software for random input and a clock cycle of 10 μs period. Figure (5.4) shows the results of the simulation. In the same time, the same data were entered to MATLAB and the standard CRC function was used with the 8-bit generator of equation (5.5). by comparing the results of the MATLAB simulation with that obtained from the ModelSim software it was found that the results were identical. This implies that the CRC8 circuit is functioning properly.

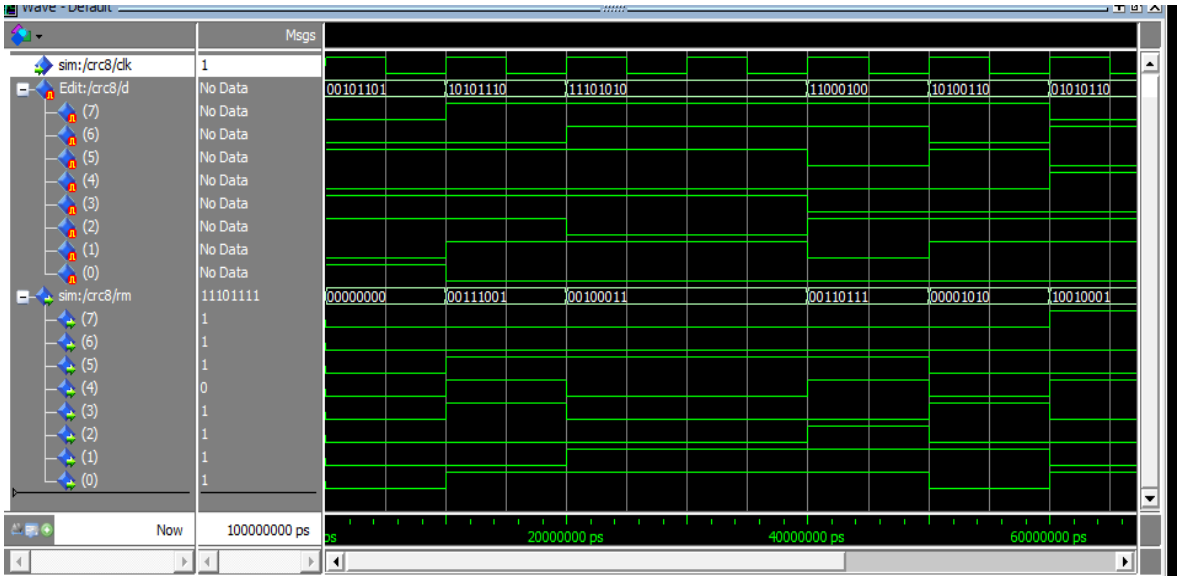


Figure (5.4): Simulation Results of the CRC8 Circuit using Altera ModelSim.

5.3.2. 16-bit CRC circuit design.

By applying equation (5.5) into equations (5.9) and choosing ω=16, F^{16} is given in hexadecimal form as:

$$F^{16} = [0C88 \quad 0644 \quad 0322 \quad 8191 \quad CC40 \quad 6620 \quad B310 \quad D988 \quad \dots$$

$$ECC4 \quad 7662 \quad 3B31 \quad 9110 \quad C888 \quad 6444 \quad 3222 \quad 1911]' \qquad (5.12)$$

By using equation (5.10), the circuit that represents the 16-bit CRC is shown in Figure (5.5). This circuit used 357 FPGA logic elements, and 16 dedicated registers.

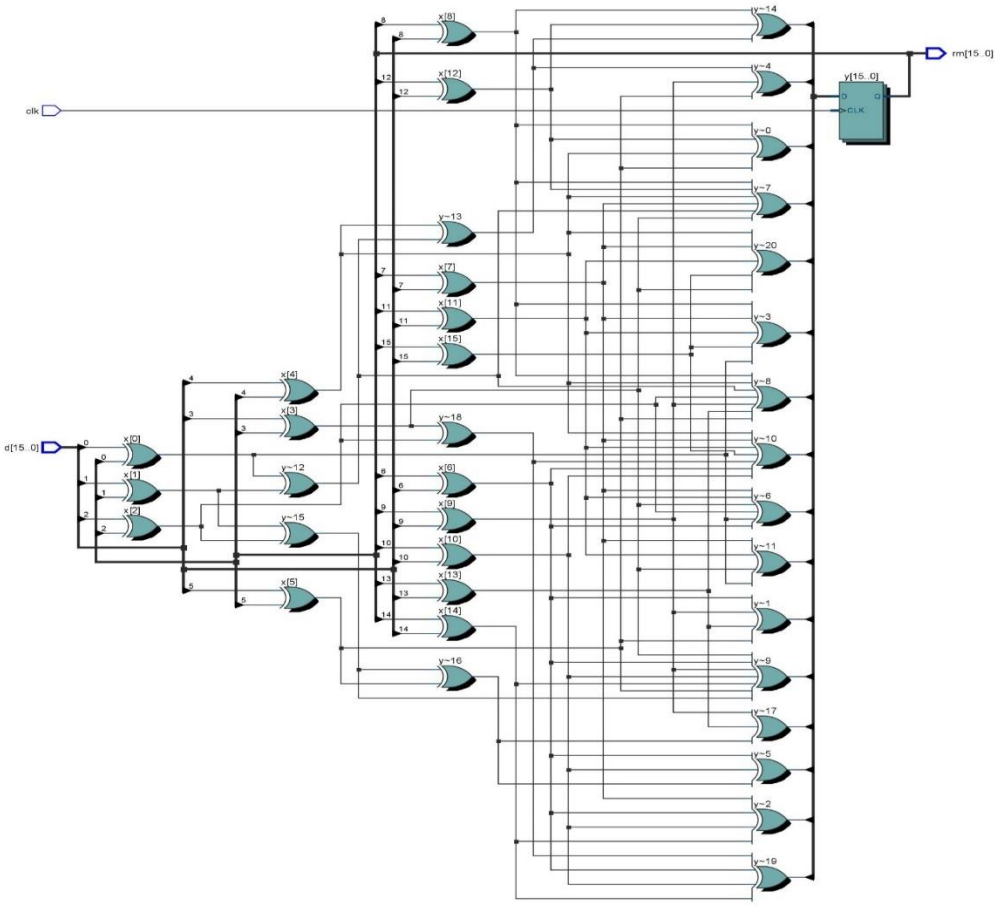


Figure (5.5): Implementation of the 16-Bit CRC Circuit.

5.3.3. 24-bit CRC circuit design.

By applying equation (5.3) into equations (5.9) and choosing ω=24, F^{24} is given in hexadecimal form as:

$$F^{24} = [C1FFFF \quad 210000 \quad 108000 \quad 084000 \quad 042000 \quad 021000 \quad 010800 \quad 008400 \quad \dots$$
$$004200 \quad 002100 \quad 001080 \quad 000840 \quad 800420 \quad 400210 \quad 200108 \quad 100084 \quad \dots$$
$$080042 \quad 040021 \quad C3FFEF \quad 200008 \quad 100004 \quad 080002 \quad 840001 \quad 83FFFF]' \tag{5.13}$$

By using equation (5.10) the circuit that represents the 24-bit CRC is shown in Figure (5.6). This circuit used 36 logic elements, and 24 dedicated registers.

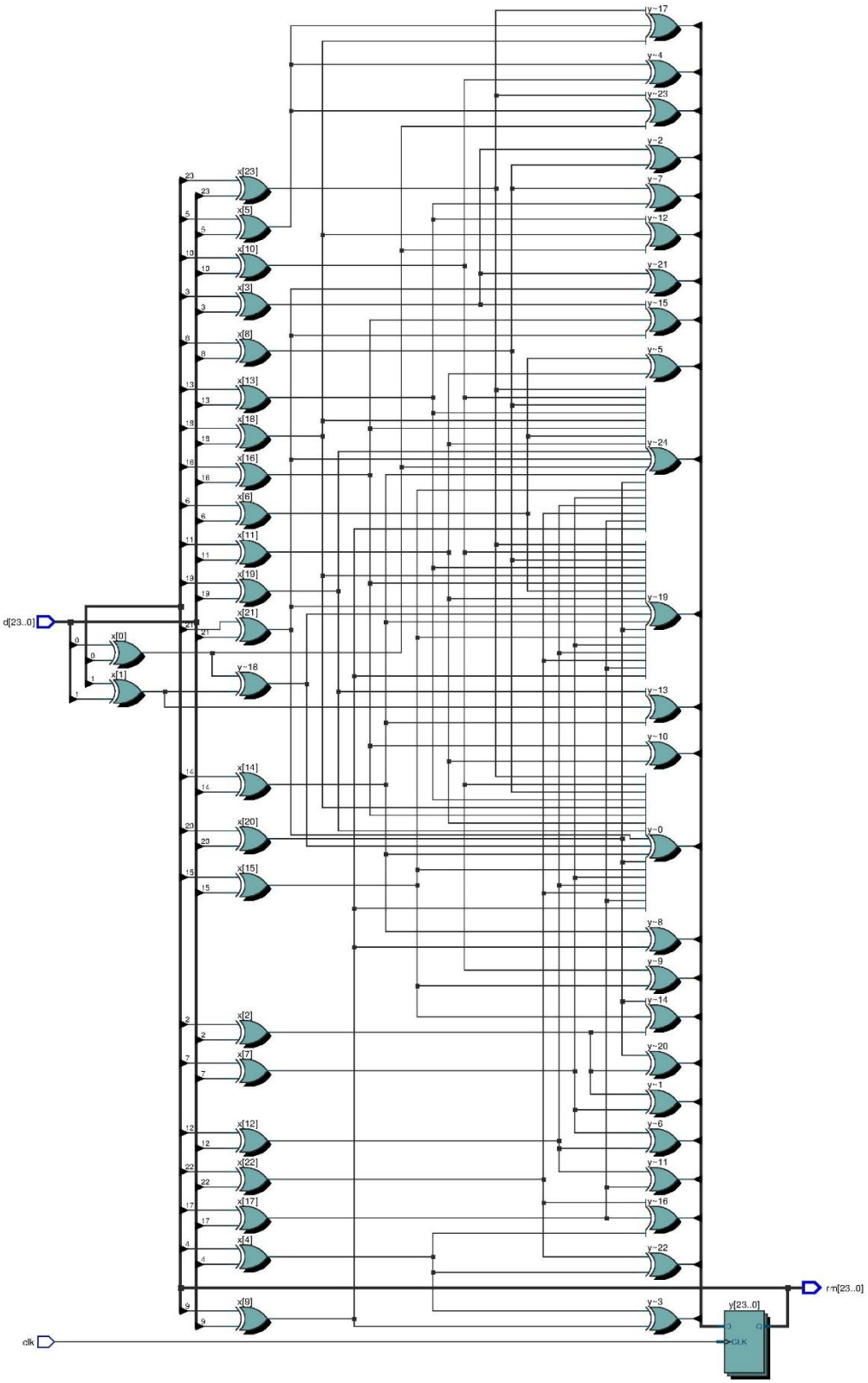


Figure (5.6): Implementation of the 24-Bit CRC Circuit.

5.4. MULTI-POLYNOMIAL CRC CIRCUIT DESIGN ALGORITHM.

Equations (5.9) and (5.10) give a general format for the LFSR for any CRC generator, but it is worth noting that once the generator is selected, F^{ω} is fixed and it cannot be altered. At the same time, the number of bits this system uses is fixed by the designer (i.e. the input buffer size to the system is fixed).

In LTE, four different types of polynomial are used, each of a different data size (8, 16, and 24). A circuit that can generate CRC from the set of equations of (5.3), (5.4), and (5.5) is needed. One solution is to implement each circuit separately and combine them in one architecture, but that will increase the used area. Another solution is to combine all the needed polynomials in one circuit to generate the desired CRC when needed. The second solution is discussed below.

Before discussing the proposed algorithm to generate the multi polynomial algorithm, the following points should be considered:

1. As mentioned in section (5.3), the algorithm will not include g_{CRC24A} because it can be calculated in parallel with g_{CRC24B} if needed. Therefore, the algorithm will target only g_{CRC24B}, g_{CRC16}, and g_{CRC8}.
2. Data buffer that holds the data, and the buffer that hold the remainder, have the same size as the generator itself (e.g. for g_{CRC16}, the buffer size is 16 bit), that is, the output data size is the same for each polynomial.

Due to point 2 above, the system should produce 24 bits' remainder for g_{CRC24B}, 16 bits remainder for g_{CRC16}, and 8-bit remainder for g_{CRC8}.

A suggestion that F^{ω} should work as a selector for the XOR gate is given in (Campobello et al., 2003). Hence, three matrices were generated using the method discussed in section 5.3, which are: $F_{CRC8}{}^{8}$, $F_{CRC16}{}^{16}$, and $F_{CRC24}{}^{24}$. After that, it was noticed that each polynomial will affect a certain number of bits and its effect will not extend to other bits in the system. In other words, if a 24×24-bit F matrix is used, an 8×8-bit F matrix can be merged with it if it is positioned correctly (in this case the upper left-hand side of the 24×24 matrix). The general matrix F^{T} is the merging result of $F_{CRC8}{}^{8}$,

F_{CRC16}^{16}, and F_{CRC24}^{24}. Figure (5.6) shows how the matrices are arranged in one big matrix.

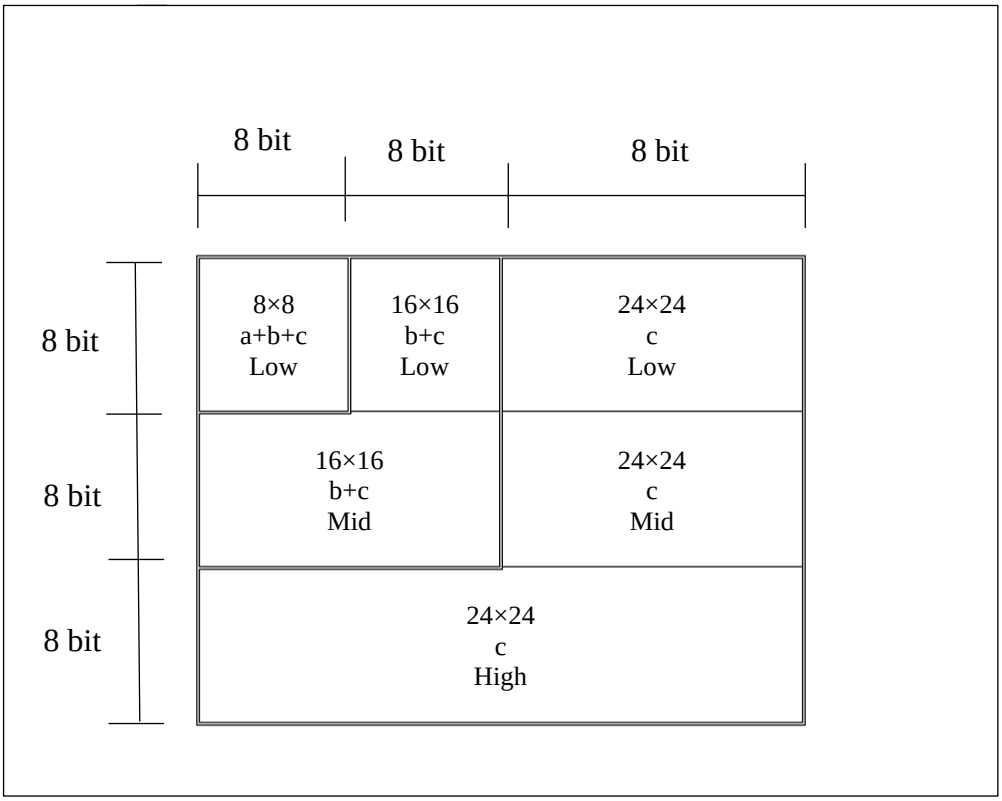


Figure (5.7): Combining F_{CRC24}^{24}, F_{CRC16}^{16}, and F_{CRC8}^{8}.

Figure (5.7) shows that the first row (8 bits) is responsible for calculating the first (low) byte of the remainder and it can be seen that the row is divided into three areas. The first is to calculate g_{CRC8}, the second will be XORed with the first area to calculate the first byte of g_{CRC16}, while the third is XORed with the first and the second areas to calculate the first byte of g_{CRC24}. The second row contain two areas that are responsible for calculating the second (mid) byte of the remainder. The first area in the second row corresponds to the second byte of g_{CRC16}, while the second area must be XORed with the first one to produce the mid byte of g_{CRC24}. Finally, the last row is responsible for calculating the third (high) byte of g_{CRC24}.

The reason behind organizing F^T in the manner shown in Figure (5.7) is to obtain the maximum power reduction. It is wise to put the unneeded stages into sleep mode, i.e. if g_{CRC8} is needed, then there is no need to include the low 16×16, low 24×24, mid 16×16, mid 24×24 and high 24×24 area in the calculation. Thus, it is put it into sleep mode to

reduce the consumed power. The same thing applies if g_{CRC16} is the used CRC, then low 24×24, mid 24×24, and high 24×24 areas are put into sleep mode.

The combination process for the three matrices will generate one 24×24 matrix that has control symbols instead of ones. These symbols are calculated according to the bit position in each one of the original matrices according to the truth table given in table (5.1).

It is wise to note that the effect of F_{CRC8}^{8} will not exceed its dimensions, so if an 8 bit CRC is needed, the values in region B and C should be all zeros or:

$$F_{CRC16}^{16}(i,j) = F_{CRC24}^{24}(i,j) = 0 \ \ for\ i,j = 9,10,\dots 24 \tag{5.14}$$

The same thing is true when using F_{CRC16}^{16} or:

$$F_{CRC24}^{24}(i,j) = 0 \ \ for\ i,j = 17,18\dots 24 \tag{5.15}$$

Table 5.1: Calculation of the new elements in the F^T Matrix

$FCRC^{24}(i,j)$	$FCRC^{16}(i,j)$	$FCRC^{8}(i,j)$	$F^T(i,j)$
0	**0**	**0**	**0**
0	**0**	**1**	**a**
0	**1**	**0**	**b**
0	**1**	**1**	**a+b**
1	**0**	**0**	**c**
1	**0**	**1**	**a+c**
1	**1**	**0**	**b+c**
1	**1**	**1**	**1**

The algorithm to calculate F^T is given below:

1. Calculate F_{CRC8}, F_{CRC16}, and F_{CRC24} individually.
2. For i=1 to 24 do.
3. For j=1 to 24 do.
4. If i>8 or j>8, then FCRC8 (i,j)=0.
5. If i>16 or j>16, then FCRC16 (i,j)=0.
6. Calculate F^T(i,j) as in table (5.1).

7. End

The new matrix F^T is used instead of F^{ω} in equation (5.9) to produce the desired parallel circuit.

The a, b, and c lines will decide which region of F^T matrix to use. If a is activated, then the first 8×8 square of the matrix is used. If b is activated, then the first 16×16 quarter of the F^T matrix is used, while if c is activated then the whole F^T matrix is used. This implies that one and only one of a, b, and b could be active at each time. The resulting F^T is divided into six submatrices given by:

$$low_{bit_8} = \begin{bmatrix} c & a+c & 0 & 0 & b & a+b & a & a+c \\ 0 & a & a+c & 0 & 0 & a+b & b & c \\ 0 & 0 & a & a+c & 0 & 0 & a+b & b \\ b & 0 & 0 & a & a+c & 0 & 0 & a+b \\ a+b & a+b & 0 & 0 & a+b & b+c & a & a \\ 0 & b & a+b & 0 & 0 & b & 1 & 0 \\ a+b & 0 & b & a+b & 0 & 0 & b & 1 \\ a+b & b & 0 & b & a+b & a & a & a+b \end{bmatrix} \quad \ldots(5.16)$$

$$low\_bit_{16} = \begin{bmatrix} 1 & c & c & c & 1 & c & c & c \\ 0 & b & 0 & 0 & 0 & b & 0 & 0 \\ c & 0 & b & 0 & 0 & 0 & b & 0 \\ b & c & 0 & b & 0 & 0 & 0 & b \\ 0 & b & c & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & b & c & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & b & c & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & b & c & 0 & 0 \end{bmatrix} \quad (5.17)$$

$$low\_bit_{24} = [FF \quad 00 \quad 00 \quad 00 \quad 00 \quad 00 \quad 00 \quad 00]' \quad (5.18)$$

$$mid\_bit_{16} = \begin{bmatrix} b & b & b & 0 & b & b & 0 & 0 & b & 1 & 0 & 0 & 0 & b & c & 0 \\ 0 & b & b & b & 0 & b & b & 0 & 0 & b & 1 & 0 & 0 & 0 & b & c \\ 0 & 0 & b & b & b & 0 & b & b & 0 & 0 & b & 1 & 0 & 0 & 0 & b \\ b & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 & b & c & 0 & 0 & 0 \\ 1 & b & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 \\ 0 & 1 & b & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 & b & c & 0 \\ 0 & 0 & 1 & b & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 & b & c \\ 0 & 0 & 0 & 1 & b & 0 & 0 & b & 0 & 0 & 0 & b & 0 & 0 & 0 & b \end{bmatrix} \quad \ldots(5.19)$$

$$mid\_bit_{24} = [00 \quad 00 \quad 80 \quad 40 \quad 20 \quad 10 \quad 08 \quad 84]' \quad (5.20)$$

$$high\_bit_{24} =$$

$$[080022 \quad 040021 \quad C3FFEF \quad 200008 \quad 100004 \quad 080002 \quad 840001 \quad 83FFFF]' \qquad \ldots(5.21)$$

Please note that equations (5.18) and (5.21) were written in hexadecimal form for simplicity. The resulting F^T is given by:

$$F^T = \begin{bmatrix} low\_bit_8 & low\_bit_{16} & low\_bit_{24} \\ & mid\_bit_{16} & mid\_bit_{24} \\ & & high\_bit_{24} \end{bmatrix} \qquad (5.22)$$

Each one of equations (5.16), (5.17), (5.18), (5.19), (5.20), and (5.21) is represented in a circuit. These circuits are shown in Figure (5.8) for the low_bit_8, Figure (5.9) for low_bit_{16}, Figure (5.10) for low_bit_{24}, Figure (5.11) for mid_bit_{16}, Figure (5.12) for mid_bit_{24}, and Figure (5.13) for $high\_bit_{24}$.

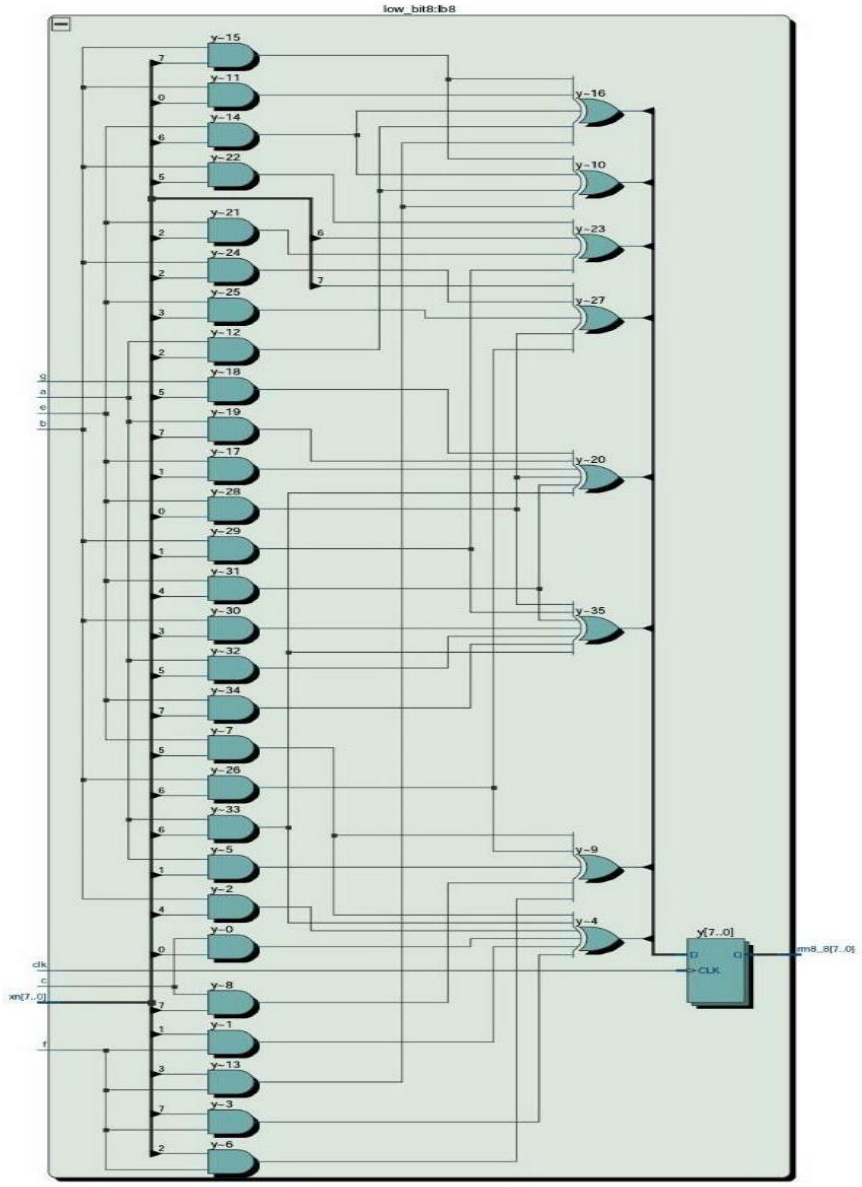


Figure (5.8): low_bit$_8$ Digital Circuit.

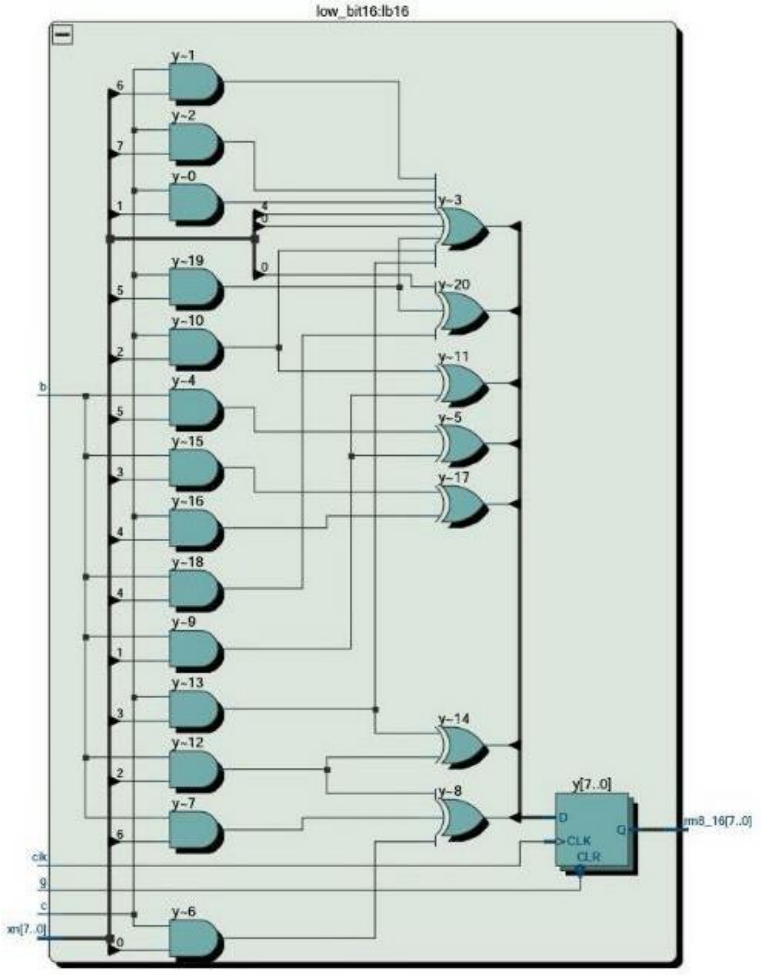


Figure (5.9): low_bit$_{16}$ Digital Circuit.

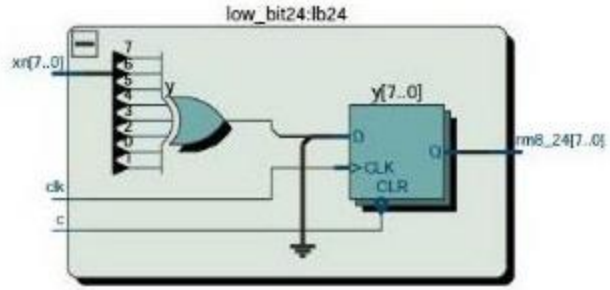


Figure (5.10): low_bit$_{24}$ Digital Circuit.

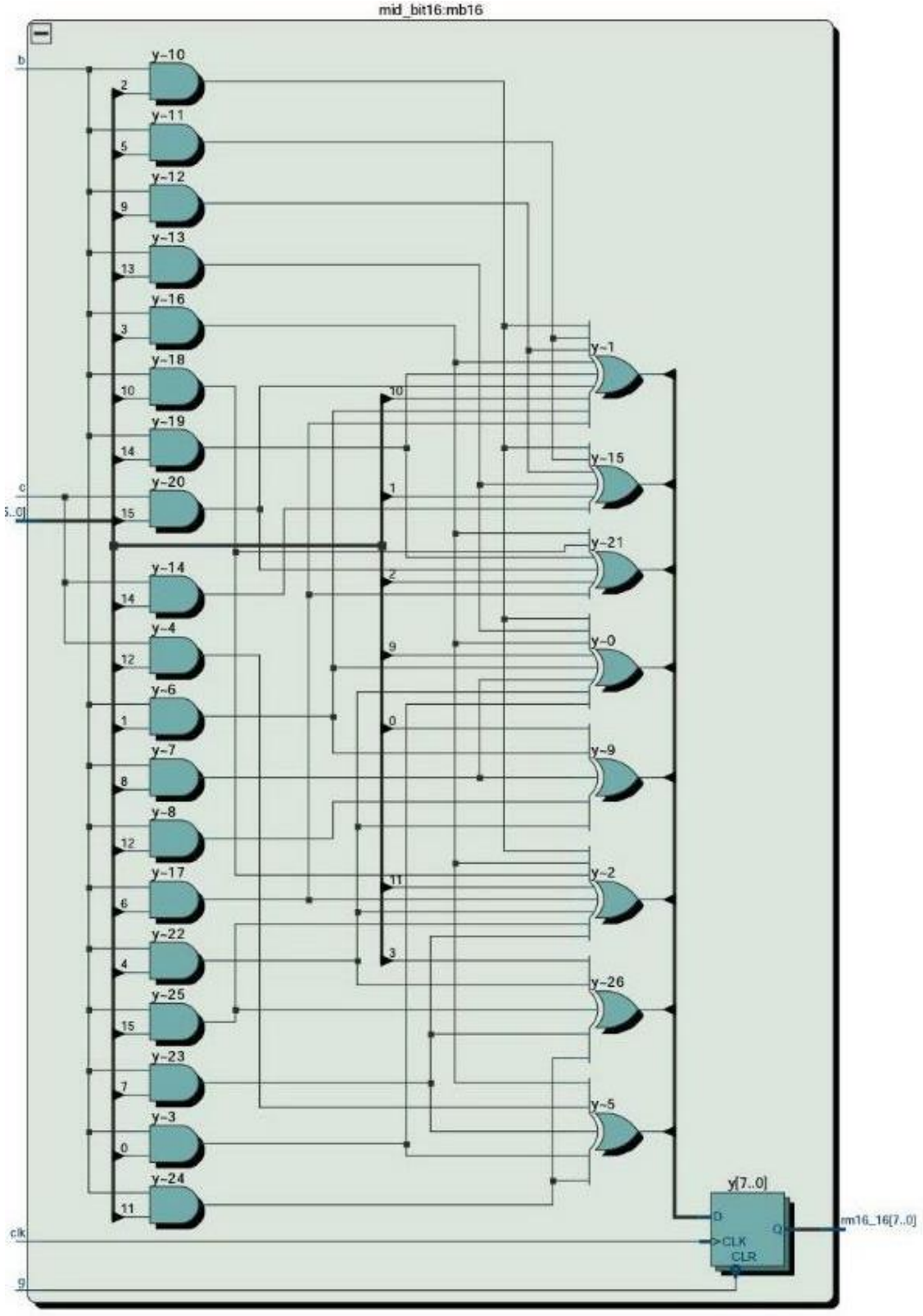


Figure (5.11): mid_bit$_{16}$ Digital Circuit.

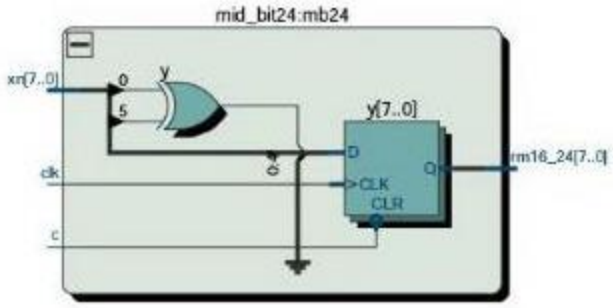


Figure (5.12): mid_bit$_{24}$ Digital Circuit.

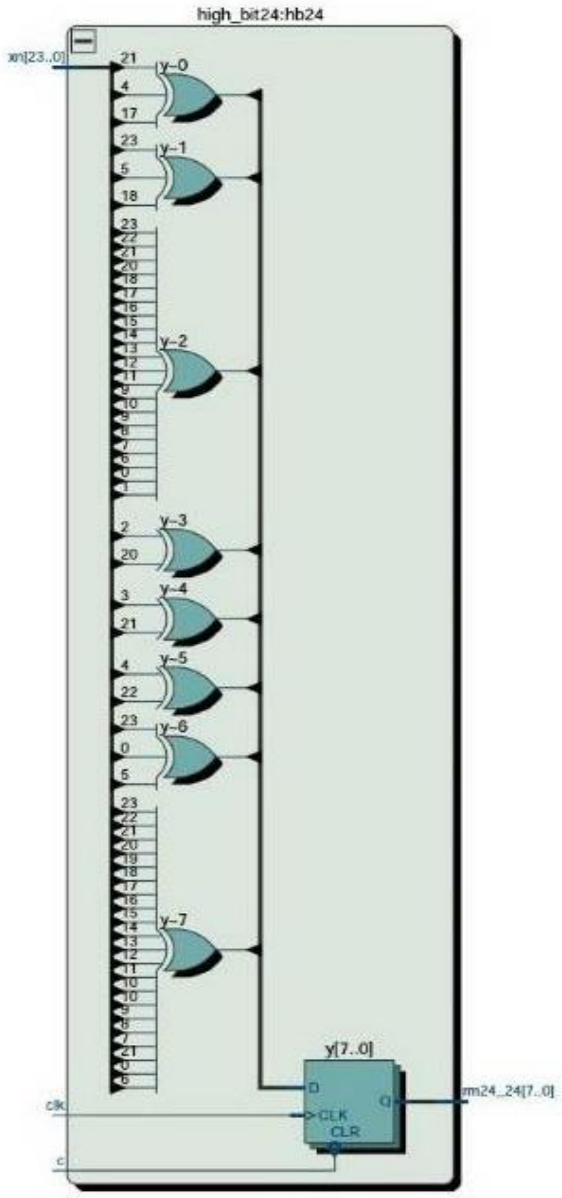


Figure (5.13): high_bit$_{24}$ Digital Circuit.

5.5. IMPLEMENTATION AND RESULTS OF THE MULTI CRC CIRCUITS.

Two systems were built to generate the required CRC remainder for the LTE system. The systems used in this test are the ordinary three CRC circuits and the multi polynomial circuit. The purpose of the test is to choose the best system for LTE from the power consumption point of view. The test was carried out to measure the throughput and the power consumption of the system. The implementation used the Terasic DE4 board based on the Altera Startix IV FPGA (Terasic, n.d.).

5.5.1. Three CRC System.

The three CRC circuit is based on equations (5.11), (5.12), and (5.13). It uses the circuits of Figures (5.3), (5.5), and (5.6) to generate the required remainder. The full circuit is shown in Figure (5.14).

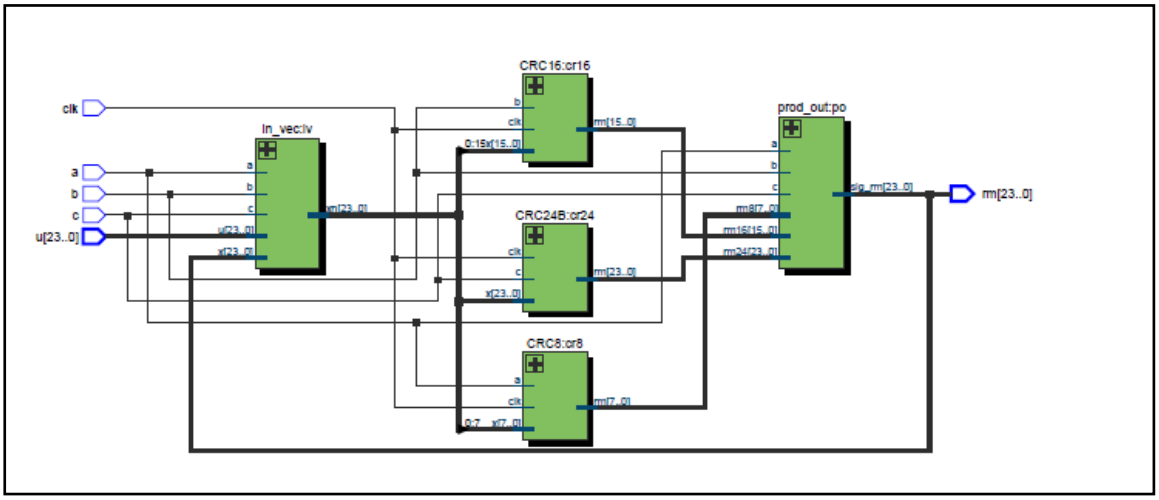


Figure (5.14): The Three CRC Circuit.

The inputs to the system are the clock (clk), the selection lines (a,b and c), and the input data (u) while the output is the remainder (rm) which is feedback to in_vec to provide the current state x(k) in the next clock cycle. The first stage in Figure (5.14) is in_vec which will decide the input vector size according to the selection lines and produce the needed input to the CRC stages from both the input vector u[24…0] and the previous remainder rm[24…0]. The next six blocks are the logic circuits that represent the F^T. The final stage is prod_out which will produce the desired output from the system by XORing the remainders corresponding to each CRC generator to give the final result which is fed to the output and to in_vec as a feedback signal.

The used circuit in in_vec and prod_out are shown in Figures (5.15) and (5.16) respectively.

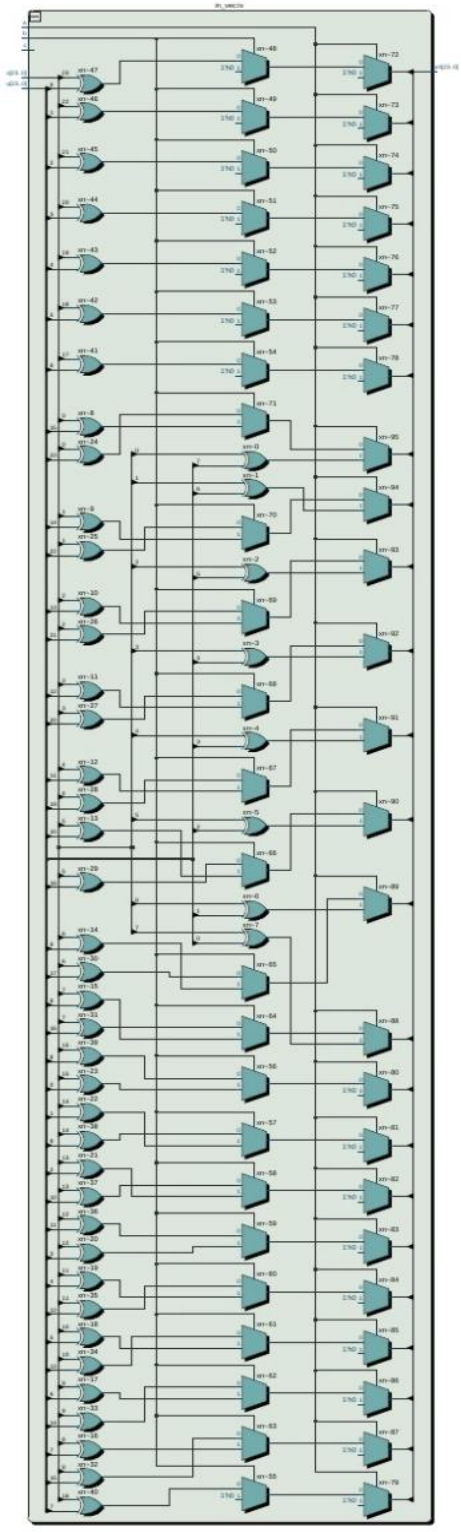


Figure (5.15): The in_Vec Circuit of the Three CRC Circuit.

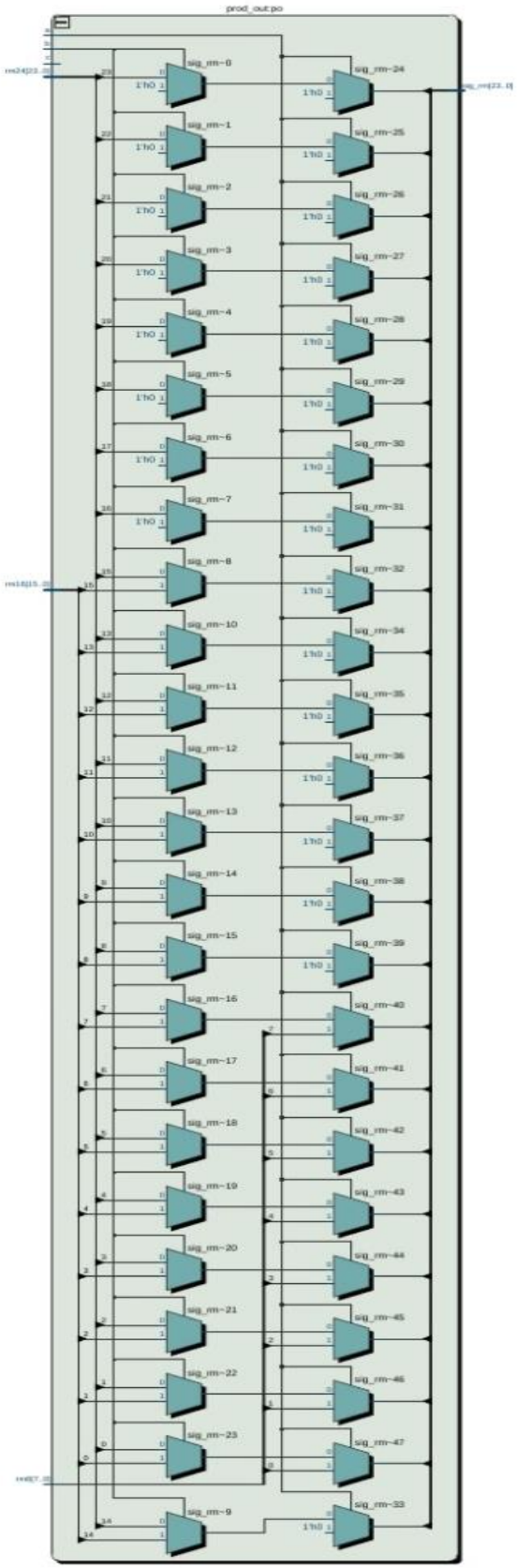


Figure (5.16): The Prod_out Circuit of the Three CRC Circuit.

Compiling the circuit using Quartus II software produced the following facts: the total logic elements used is 137, and total number of used registers is 48.

5.5.2. Multi-Polynomial CRC Circuit.

The multi-polynomial CRC circuit is based on equations (5.16), (5.17), (5.18), (5.19), (5.20), and (5.21). It uses the circuits of Figures (5.8), (5.9), (5.10), (5.11), (5.12) and (5.13) to generate the required remainder. The full circuit is shown in Figure (5.17).

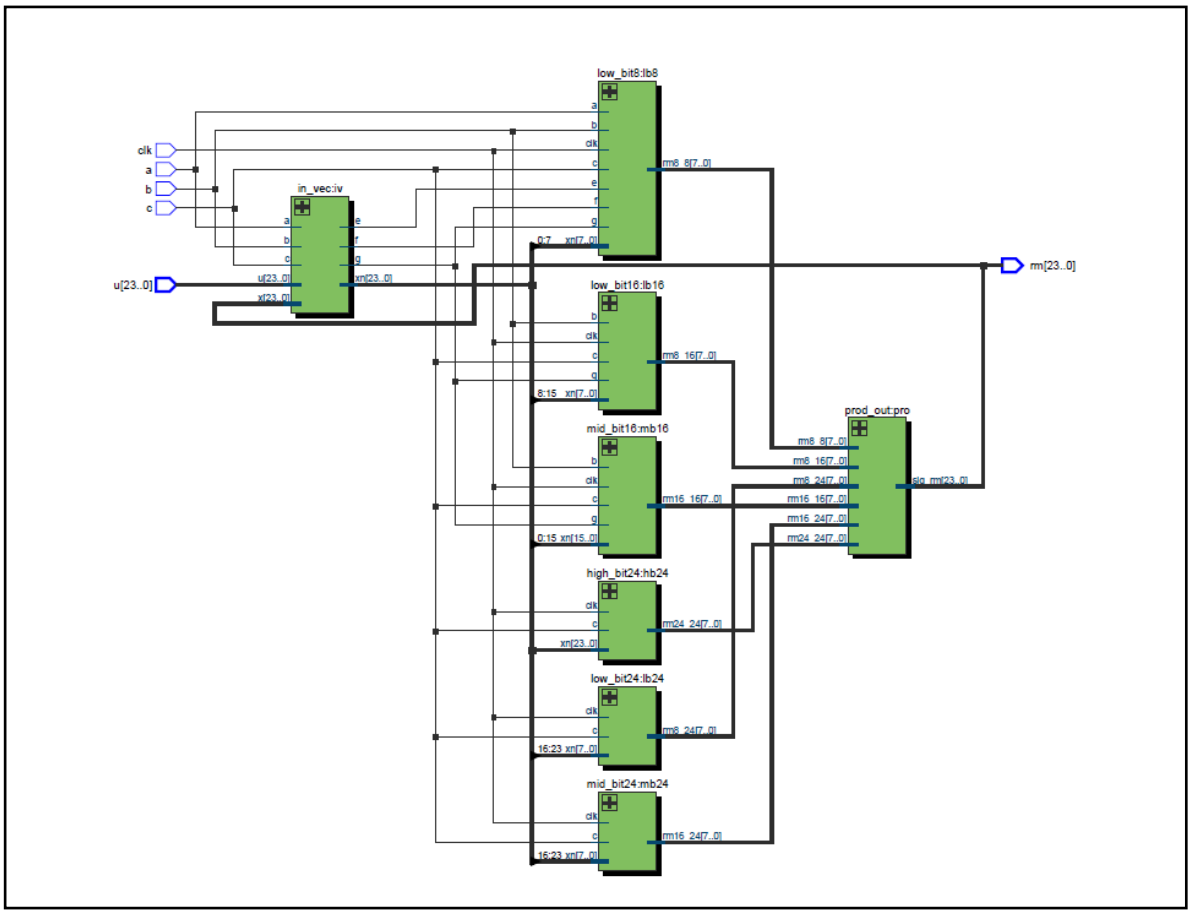


Figure (5.17): The Multi-Polynomial CRC Circuit.

The inputs to the system are the clock (clk), the selection lines (a,b and c), and the input data (u) while the output is the remainder (rm). The first stage in Figure (5.17) is in_vec which will decide the input vector size according to the selection lines and produce the needed input to the CRC stages from both the input vector and the previous remainder. The next six blocks are the logic circuits that represent the F^T. The final stage is prod_out which will produce the desired output from the system by XORing the remainders corresponding to each CRC generator to give the final result which is fed to the output and to in_vec as a feedback signal. The used circuit in

in_vec and prod_out in the multi-polynomial circuit are shown in Figures (5.18) and (5.19) respectively.

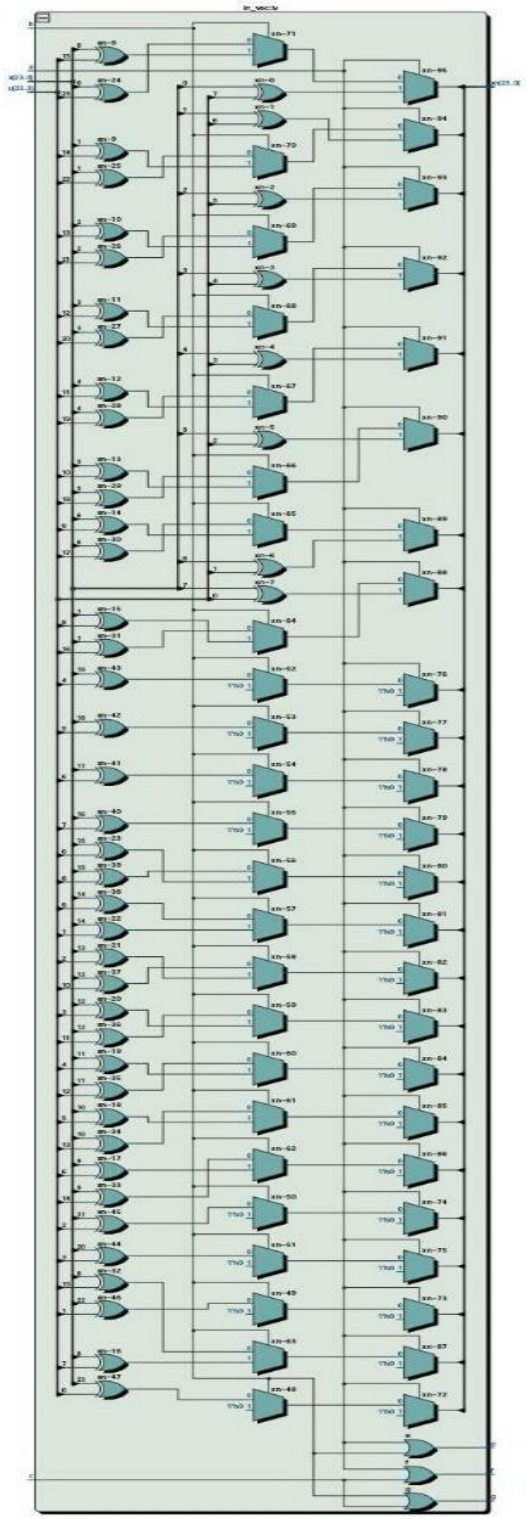


Figure (5.18): The in_Vec Circuit of the Multi-Polynomial CRC Circuit.

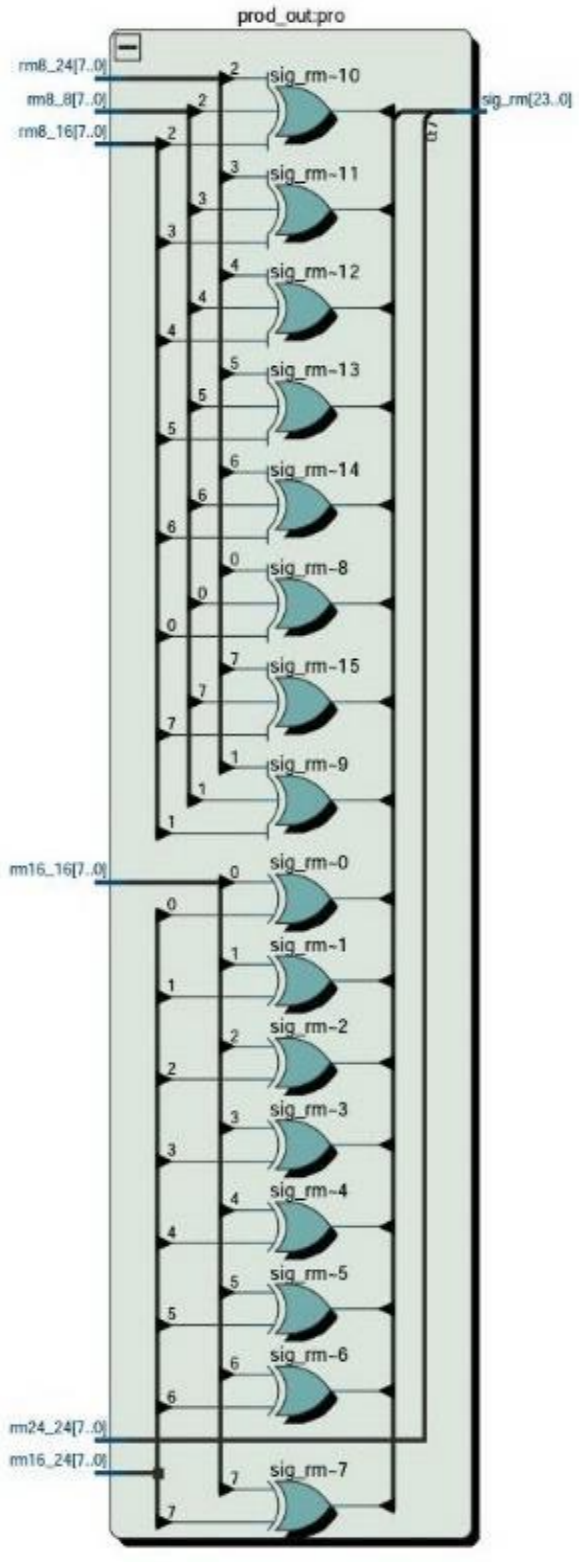


Figure (5.19): The prod_out Circuit of the Multi-Polynomial CRC Circuit.

Compiling the circuit using Quartus II software produced the following facts: the total logic elements used is 90, and total number of used registers is 24.

5.5.3. A Comparison between the Two CRC Circuits.

A simulation was carried out on Quartus II software with a clock frequency of 100 MHz which gives a throughput of 800 Mbps for g_{CRC8}, 1.2 Gbps for g_{CRC16} and 1.8 Gbps for g_{CRC24b}. The results of the simulation are shown in Table (5.2), where a comparison is made between the three CRC circuit and the multi-polynomial circuit. The comparison aims to decide which circuit is better to be used in LTE system.

Table 5.2: Results of Simulation

Used method	Multi Polynomial	Three CRC	% reduction
Number of used logic units	90	137	34.3%
Number of registers	24	48	50%
Maximum number of fan out	24	48	50%
Power Consumption using CRC8 (mW)	2.78	4.17	33.33%
Power consumption using CRC16 (mW)	2.97	4.46	33.41%
Power Consumption using CRC24B (mW)	3.22	4.63	30.45%

The obtained number of logic gates and register shown in table (5.2) is less than the other method used to parallelize CRC circuit, because the method used is to combine three different CRC polynomials in one circuit. That will reduce the number of logic gates dramatically, and hence the circuit size.

The given power readings are the dynamic power consumption by the system and this clearly shows the superiority of the proposed system in reducing the power.

The reduction in the number of logic gates and power comes from the fact that the design was made to combine three circuits in one, so the total number of logic gates should be less than that of the sum of three circuits together. As an example (Cheng & Parhi, 2006) designed g_{CRC16} with only 80 logic gates, while in this method 90 gates can produce the remainder for 8, 16 and 24 bits without the need for reconfiguring the circuit.

The design managed to produce the remainder bits associated with g_{CRC8}, g_{CRC16} and g_{CRC24} directly by activating the a, b or c lines without the need to load a different matrix, change

the configuration or change the data path of the incoming data, which reduces the time needed to calculate the remainder.

To observe the behaviour of the circuits towards the change in frequency, a setup was prepared using Quartus II programme with the aid of Power Play Power Optimizer tool. The setup aims to measure the power of the multi-polynomial circuit with different frequencies and at the same time calculate the throughput of the system. It is very important to note that the maximum frequency reached, and hence the throughput, should not conflict with the critical path time, so that data integrity is not touched. The critical path time is the maximum time that the input needs to propagate through the circuit (T_{max}).

The simulation result is shown in table (5.3) where the frequency was chosen in the range of 10-200 MHz with 10 MHz steps. The data are plotted in Figure (5.20) and the relation between power and frequency is clearly linear. Another important feature to be seen in table (5.3) is that for LTE systems, where a throughput of 1 Gbit/sec is needed (3GPP Specifications, 2015b), the required frequency for operation is 130 MHz for CRC8, 70 MHz for CRC16 and 50 MHz for CRC24. That is, the system will consume 3.64 mW, 2.09 mW and 1.53 mW corresponding to CRC8, CRC16 and CRC24 respectively, while it can consume 2.78 mW, 2.97 mW, and 3.22 mW for the same CRCs whilst working in a constant 100 MHz frequency. The reduction in power according to this technique is -30.94%, 29.6%, and 52.48% corresponding to CRC8, CRC16, and CRC24. These results are shown in Figure (5.21). It is noted that the reduction in the power for the case of CRC8 is negative because the frequency is increased rather than decreased to maintain a constant throughput.

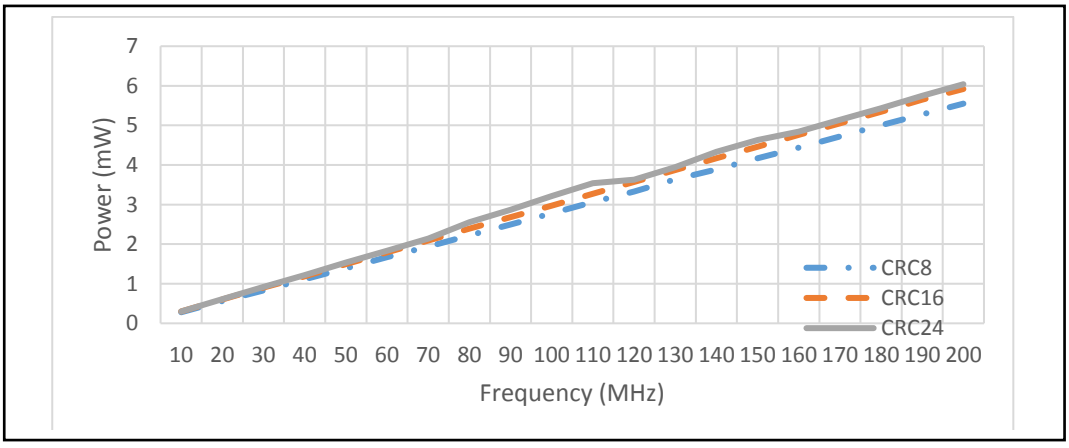


Figure (5.20): Power Consumption of CRC8, CRC16, and CRC24 Corresponding to Frequency.

Table 5.3: Power and Throughput of the proposed Circuit.

Frequency (MHz)	CRC8		CRC16		CRC24	
	Power (mW)	Throughput (Mbit/sec)	Power (mW)	Throughput (Mbit/sec)	Power (mW)	Throughput (Mbit/sec)
10	0.28	80	0.3	160	0.3	240
20	0.56	160	0.6	320	0.61	480
30	0.83	240	0.9	480	0.92	720
40	1.11	320	1.19	640	1.22	960
50	1.39	400	1.49	800	1.53	1200
60	1.67	480	1.79	960	1.83	1440
70	1.94	560	2.09	1120	2.14	1680
80	2.22	640	2.39	1280	2.55	1920
90	2.5	720	2.68	1440	2.87	2160
100	2.78	800	2.97	1600	3.22	2400
110	3.06	880	3.27	1760	3.54	2640
120	3.33	960	3.57	1920	3.63	2880
130	3.64	1040	3.87	2080	3.94	3120
140	3.89	1120	4.17	2240	4.33	3360
150	4.17	1200	4.46	2400	4.63	3600
160	4.44	1280	4.76	2560	4.84	3840
170	4.72	1360	5.05	2720	5.14	4080
180	5.00	1440	5.34	2880	5.43	4320
190	5.28	1520	5.65	3040	5.75	4560
200	5.55	1600	5.92	3200	6.04	4800

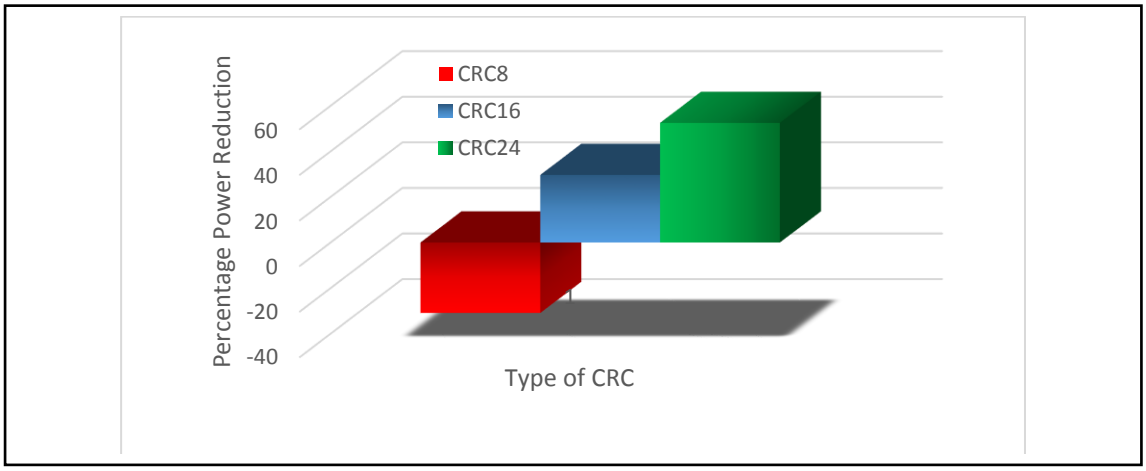


Figure (5.21): Power Reduction in the Multi-Polynomial Circuit due to Frequency Reduction.

5.6. CONCLUSION

CRC circuit is used in many data transmission systems. It is used in this thesis as a test bench to prove the ability of SPM to reduce power in communication systems. The method of designing the CRC circuit was discussed in this chapter. A parallel configuration for the 8, 16, and 24 bit CRC circuit was introduced so that it could be used later to test the SPM unit. A multi-polynomial algorithm was proposed to produce one circuit that can generate the required remainder using different CRC polynomials. The algorithm was used to build a multi-polynomial circuit that can work for the LTE standard. The new circuit can produce the remainder of the CRC8, CRC16, and CRC24 generators. The new circuit was compared to a three CRC circuit that could produce the LTE needed remainder. The test shows that the proposed multi-polynomial circuit has a fewer number of gates and registers. This feature makes the multi-polynomial CRC circuit consume less power. Another important design feature used in this circuit is the use of sleep technique. The multi-polynomial circuit divided the CRC matrix into regions each associated with certain CRC. So, if the region is not needed, it could be put into sleep state to reduce power. The results of the setup showed that for a constant frequency, the multi-polynomial circuit can reduce the power in no less than 30% over the three CRC circuit. Another setup showed that by reducing the frequency of the circuit, a considerable amount of power could be reduced provided that the throughput is intact.

In the next chapter, SPM is used in a digital communication system to control the power of a CRC circuit. The CRC8 CRC16 and CRC24 are simulated using the new power algorithm discussed in chapter two, and then SPM is used to control their power.

CHAPTER SIX

IMPLEMENTING THE SPM ON THE CRC CIRCUIT

6.1. INTRODUCTION.

The aim of this thesis is to reduce power in digital communication systems. To do so, there must be an investigation about how the power is consumed in digital systems, how to build a mathematical model for power consumption, build a controller to manage power, and finally implement the design in a communication system. In the previous chapters, these objectives were fulfilled except for implementing SPM in a communication system. In this chapter, SPM is used to control the power consumption in the CRC circuits designed in chapter five. SPM already proved its ability to reduce power in other types of circuits in chapter four. These circuits are considered the norm of any digital communication system.

CRC does not represent a complete communication system, but it is an essential unit of it. Controlling the CRC power will prove that ability of SPM to control the power of the whole communication system since it's already done so for parts of the system.

6.2. FREQUENCY LIMITS OF THE CRC CIRCUIT.

Before implementing SPM on the CRC system, there must be a previous knowledge about the limits of the CRC circuit. There are two parameters that need to be looked at, the voltage and the time delay of the CRC circuit. If the frequency is very high and the voltage is not sufficient, then the CRC circuit will start to produce a faulty output. In another word, the circuit is in the miss pulse condition.

To observe the limitations of the CRC circuit, the same tests that were implemented in section 3.5 of this thesis are used. Unfortunately, the tests are limited to the new power model, i.e. there is no CRC simulation using OrCAD Cadence. The reason behind this is that the smallest CRC circuit used in this thesis has 8 inputs and another 8 inputs which represent the remainder feedback. The total number of inputs are 16. Hence, the number of files that need processing is $2^{16}+1$ for each voltage, frequency point. The total number of files that must be processed for this circuit is 31195612 file. This will consume a huge amount of time and computational power.

Using FPGA to measure the power of the CRC is not an option since FPGA uses Logic Elements (LE) or Look-Up Tables (LUT) rather than logic gates and that will increase power consumption dramatically.

Due to the above discussion, the only tool used in this test is MATLAB.

6.2.1. Limitation of the 8-Bit CRC Circuit.

Using the circuit described in section (5.3.1), the 8-bit CRC circuit was constructed using MATLAB. It was tested under the same conditions of section (3.4), i.e. variable f variable V_{dd} for four technology sizes: 180, 90, 45 and 22 nm. The simulation results are shown in Figure (6.1) for the power consumption of the 180nm 8 bit CRC circuit while Figure (6.2) shows the time delay of the circuit. Figure (6.3) shows the power of the 8-bit CRC circuit of 90nm size, and Figure (6.4) the corresponding time delay. For the 45nm 8-bit CRC circuit, Figure (6.5) presents the power consumption and Figure (6.6) the time delay. Power consumption and time delay of the 22nm 8-bit CRC Circuit are shown in figures (5.7) and (5.8) respectively.

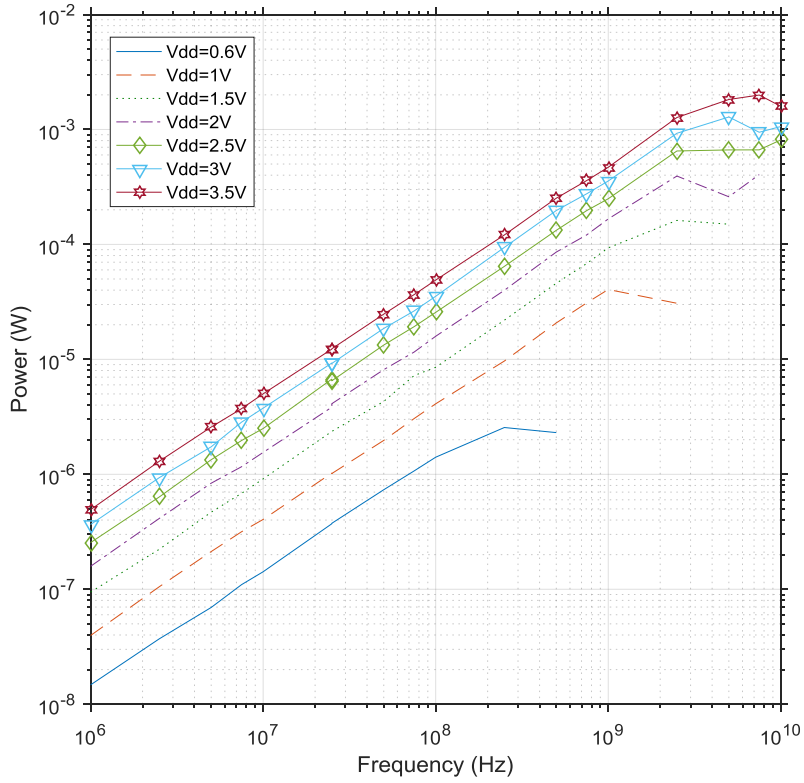


Figure (6.1): Power Consumption of an 180nm 8-Bit CRC Circuit.

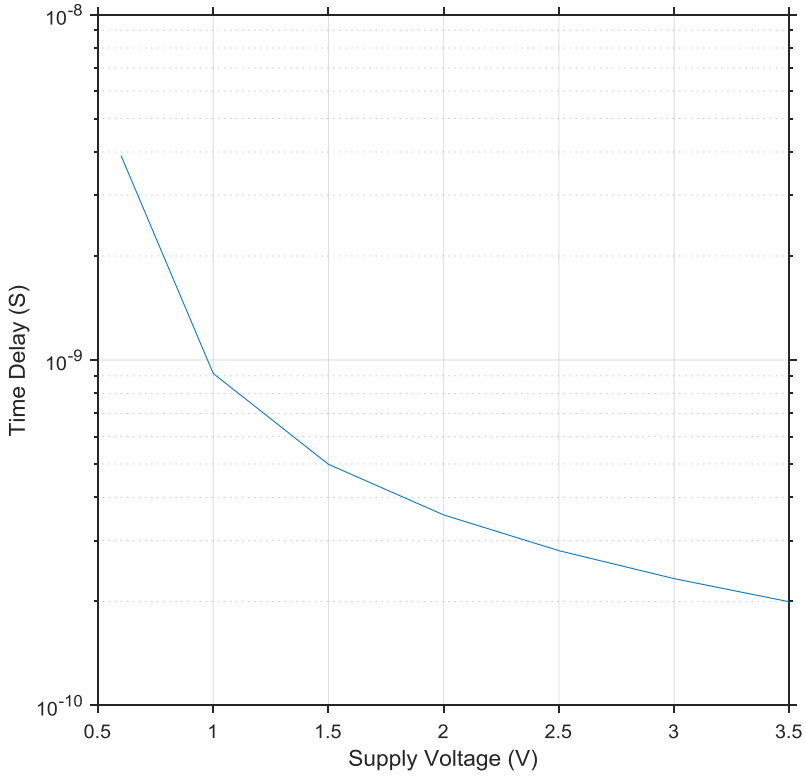


Figure (6.2): Time delay of an 180nm 8-Bit CRC Circuit.

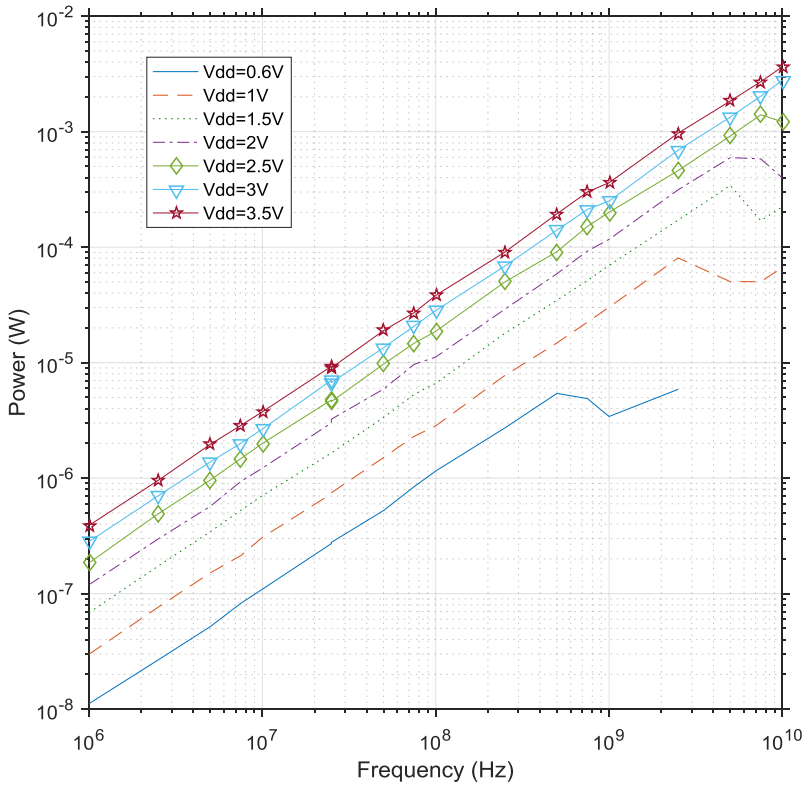


Figure (6.3): Power Consumption of a 90nm 8-Bit CRC Circuit.

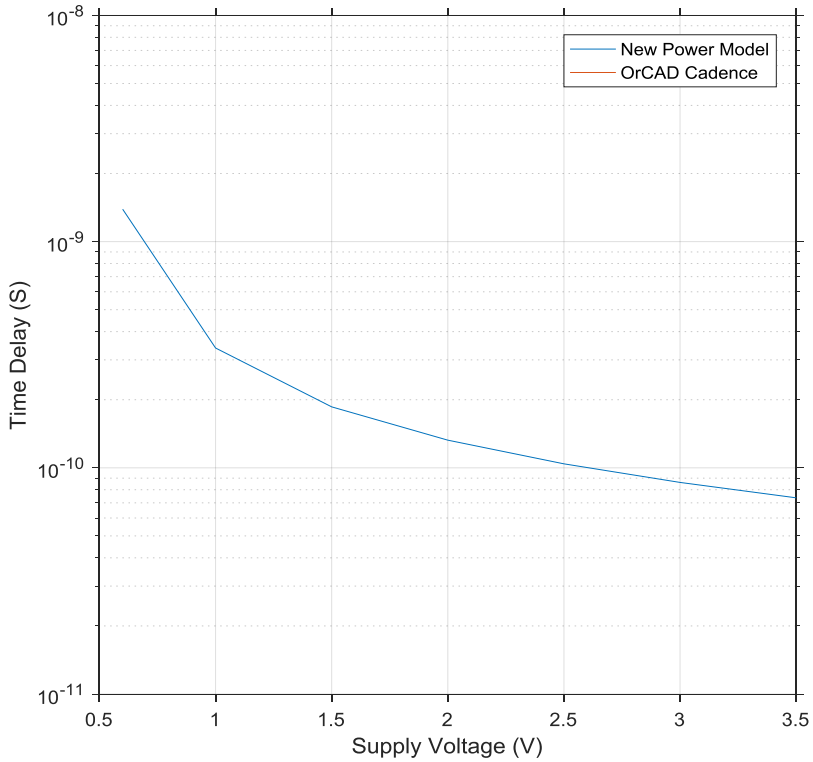


Figure (6.4): Time Delay of a 90nm 8-Bit CRC Circuit.

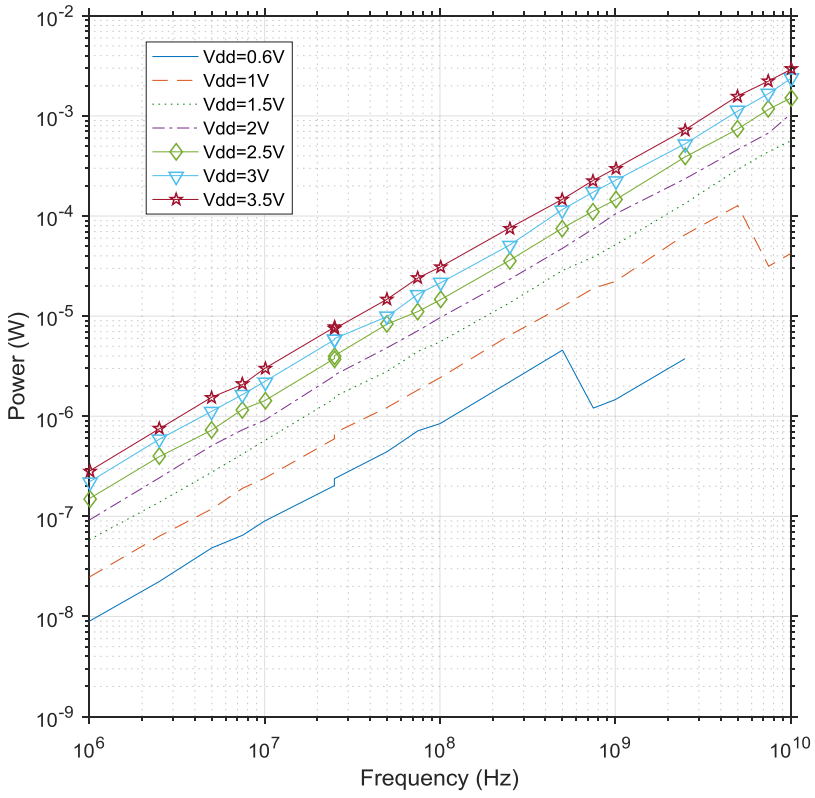


Figure (6.5): Power Consumption of a 45nm 8-Bit CRC Circuit.

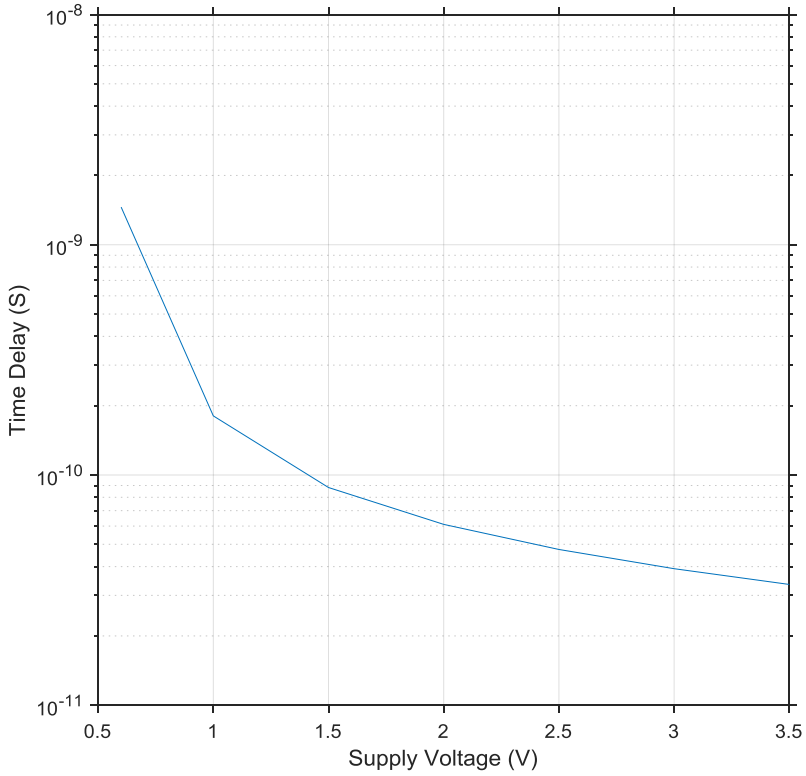


Figure (6.6): Time Delay of a 45nm 8-Bit CRC Circuit.

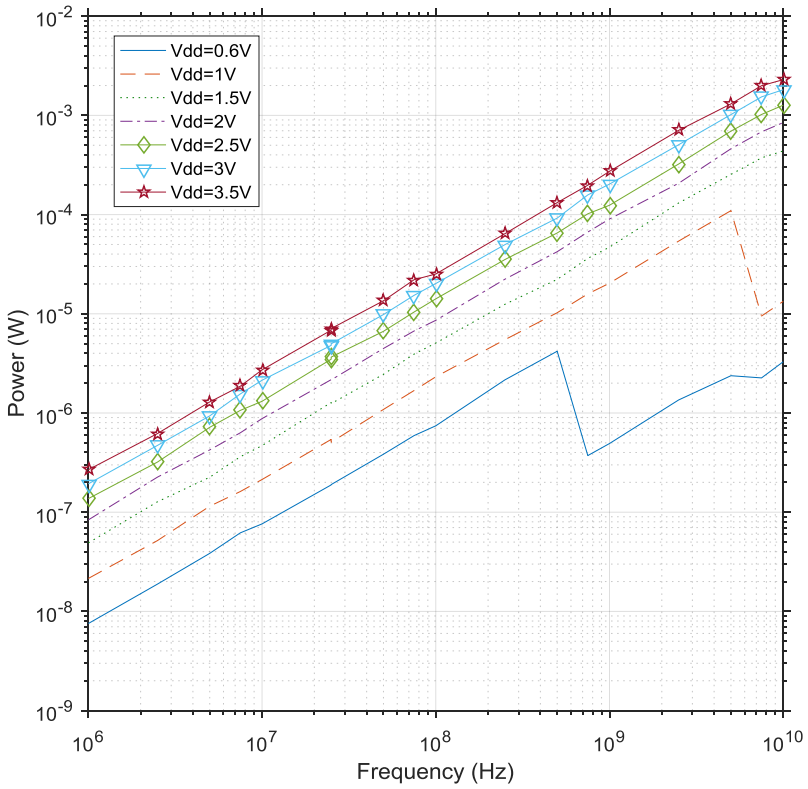


Figure (6.7): Power Consumption of a 22nm 8-Bit CRC Circuit.

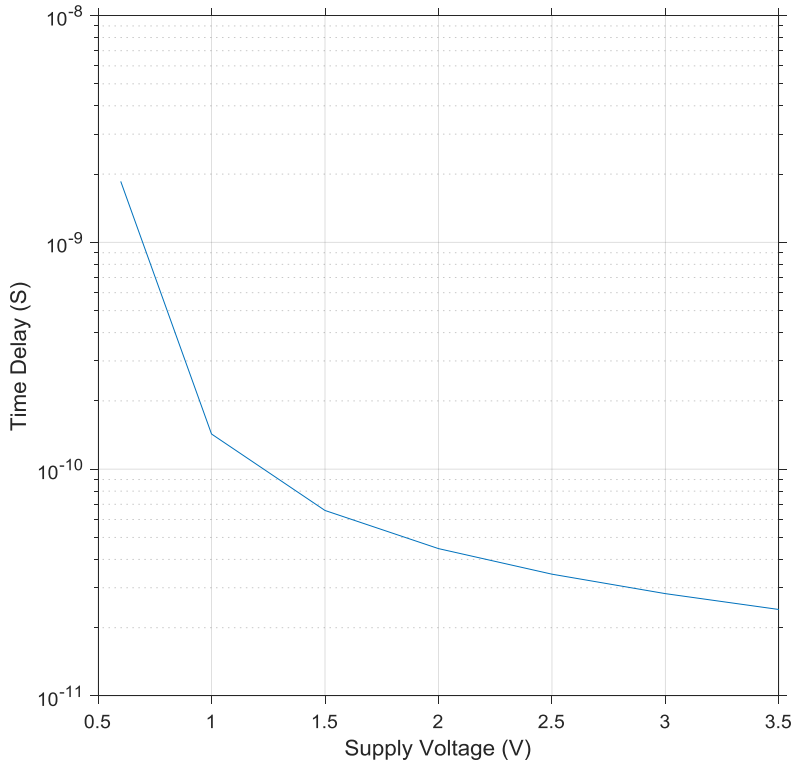


Figure (6.8): Time Delay of a 22nm 8-Bit CRC Circuit.

One can see from the Figures above that the best technology size corresponding to power is the 22nm. Furthermore using very low voltage can put the circuit into the miss pulse condition. Figures (6.2), (6.4), (6.6), and (6.8) will give the SPM the required knowledge about the time delay of the circuit so that it can check whether the voltage to be used will produce an error or not.

6.2.2. Limitation of the 16-Bit CRC Circuit.

Using the circuit described in section (5.3.2), the 16-bit CRC circuit was constructed using MATLAB. It was tested under the same conditions of section (3.4) i.e. variable frequency variable V_{dd} for four technology sizes: 180, 90, 45 and 22 nm. The simulation results are shown in Figure (6.9) for the power consumption of the 180nm 16-bit CRC circuit while Figure (6.10) shows the time delay of the circuit. Figure (6.11) presents the power of the 16-bit CRC circuit of 90nm size, and Figure (6.12) the corresponding time delay. For the 45nm 16-bit CRC circuit, Figure (6.13) shows the power consumption and Figure (6.14) the time delay. Power consumption and time delay of the 22nm 16-bit CRC Circuit are shown in figures (5.15) and (5.16) respectively.

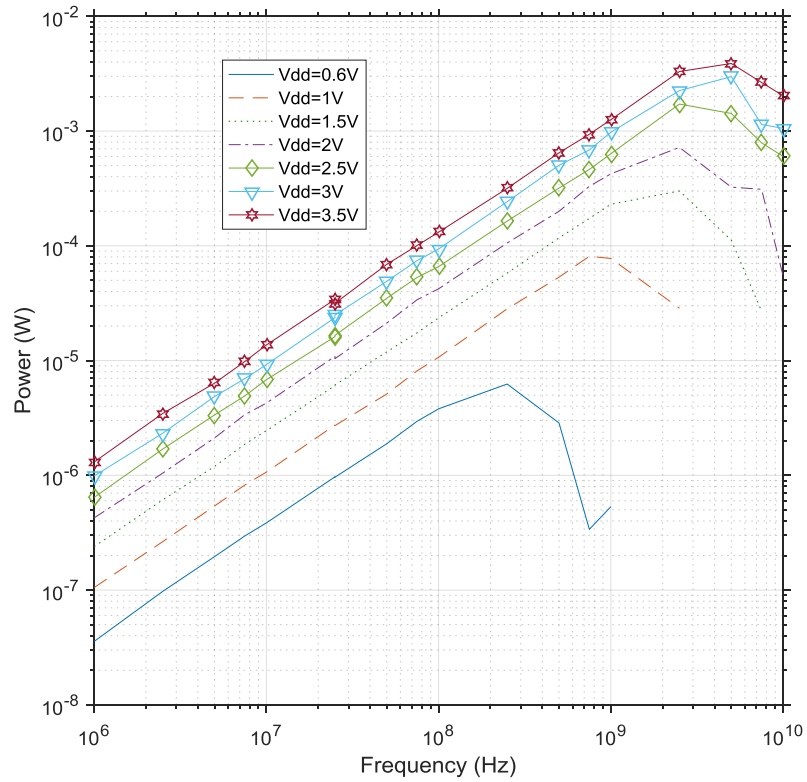


Figure (6.9): Power Consumption of an 180nm 16-Bit CRC Circuit.

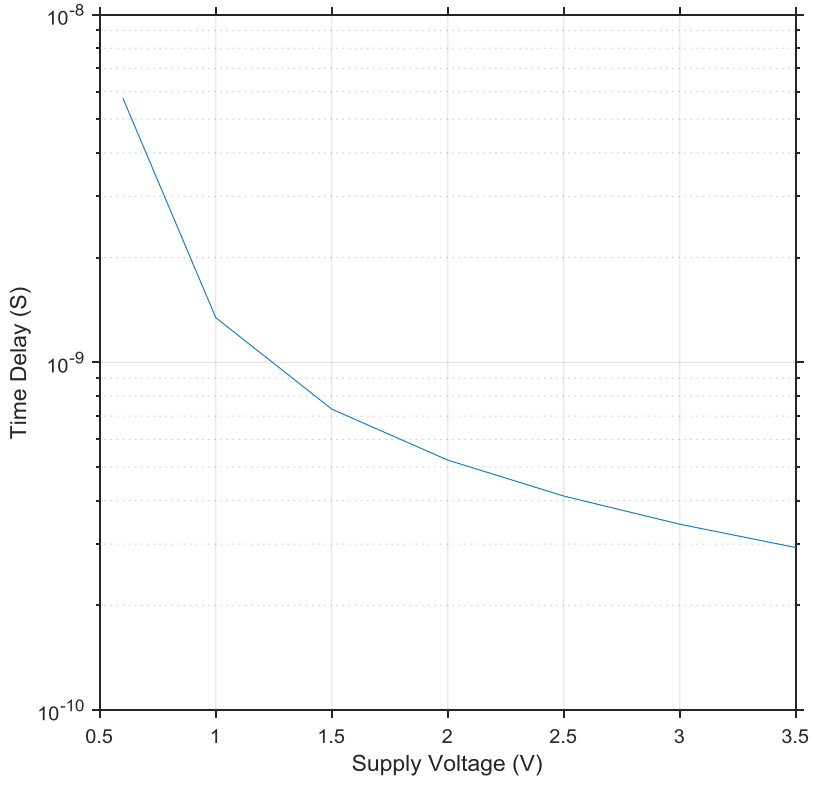


Figure (6.10): Time Delay of an 180nm 16-Bit CRC Circuit.

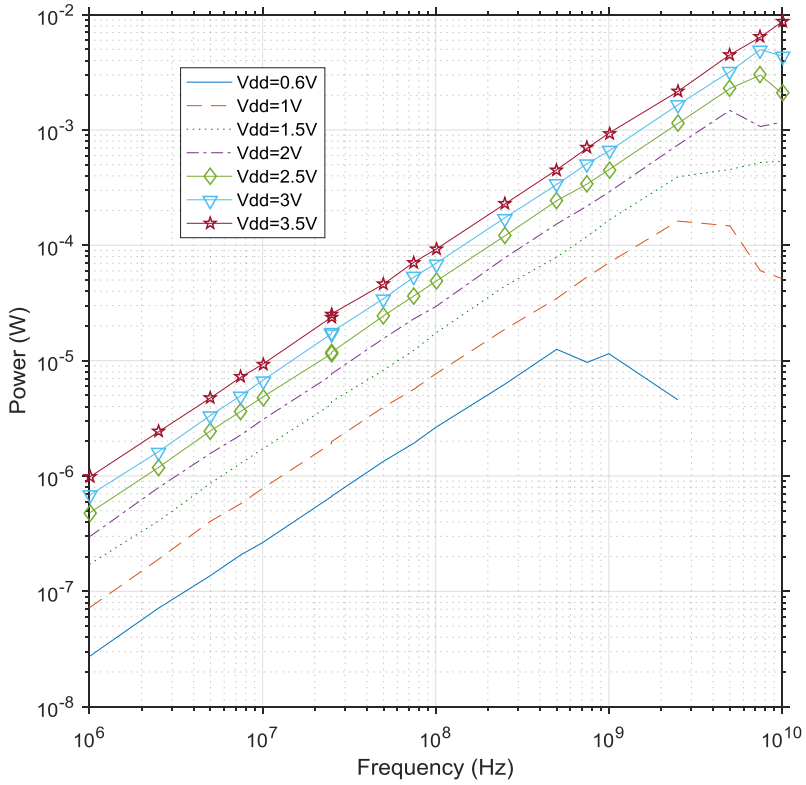


Figure (6.11): Power Consumption of a 90nm 16-Bit CRC Circuit.

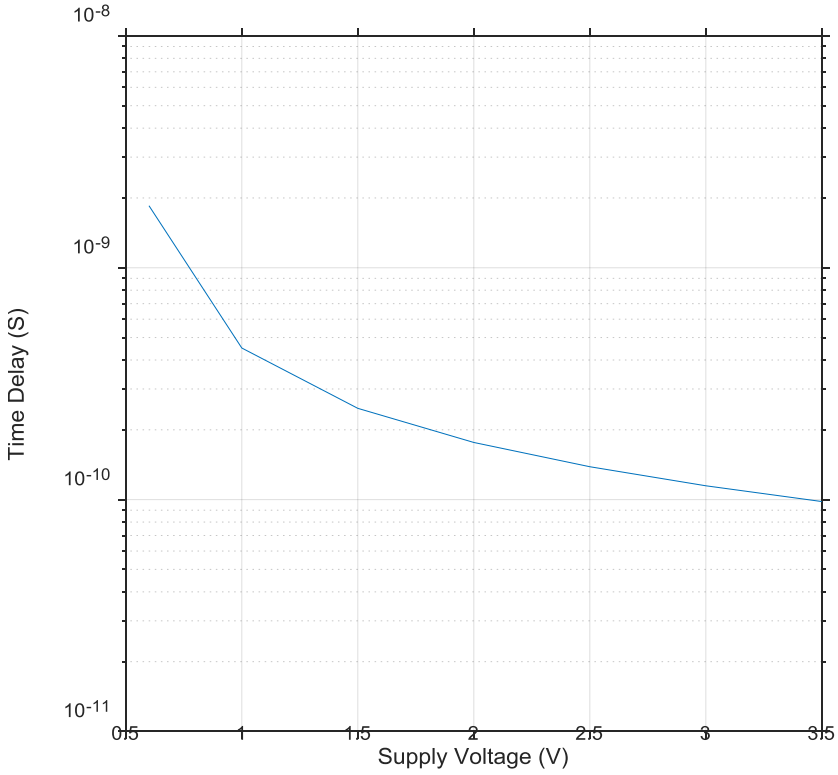


Figure (6.12): Time Delay of a 90nm 16-Bit CRC Circuit.

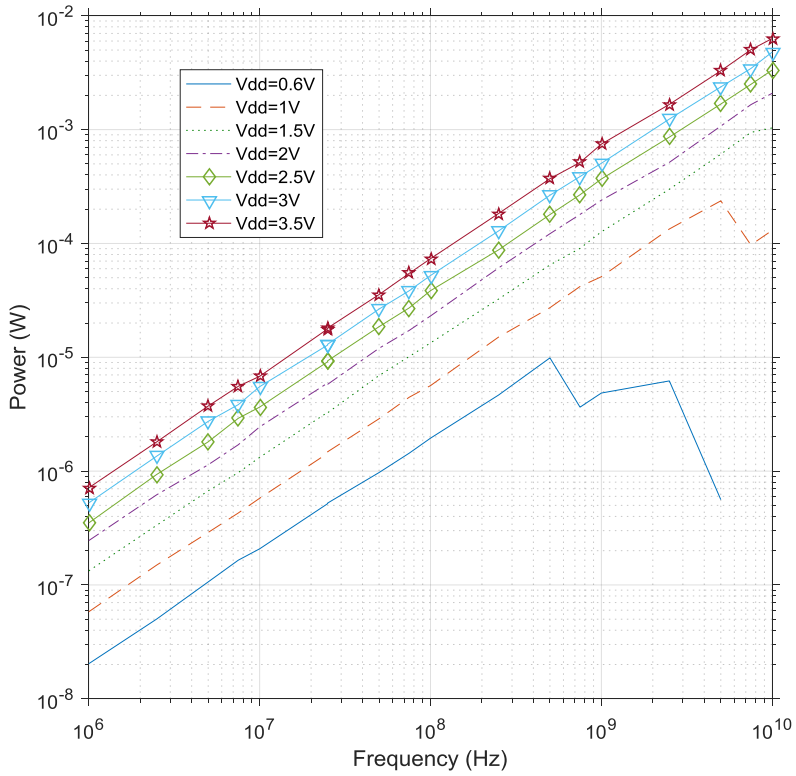


Figure (6.13): Power Consumption of a 45nm 16-Bit CRC Circuit.

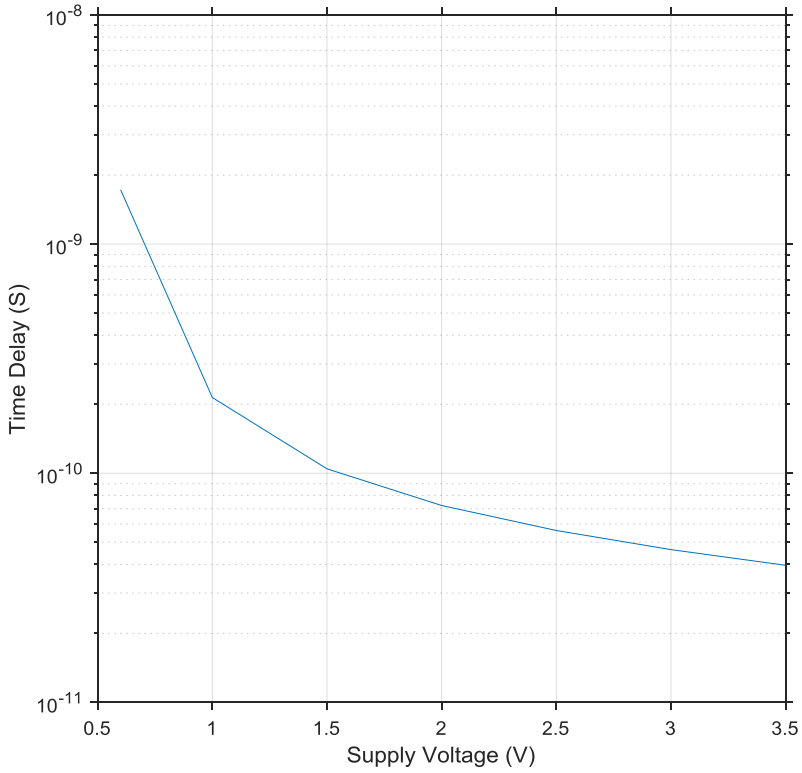


Figure (6.14): Time Delay of a 45nm 16-Bit CRC Circuit.

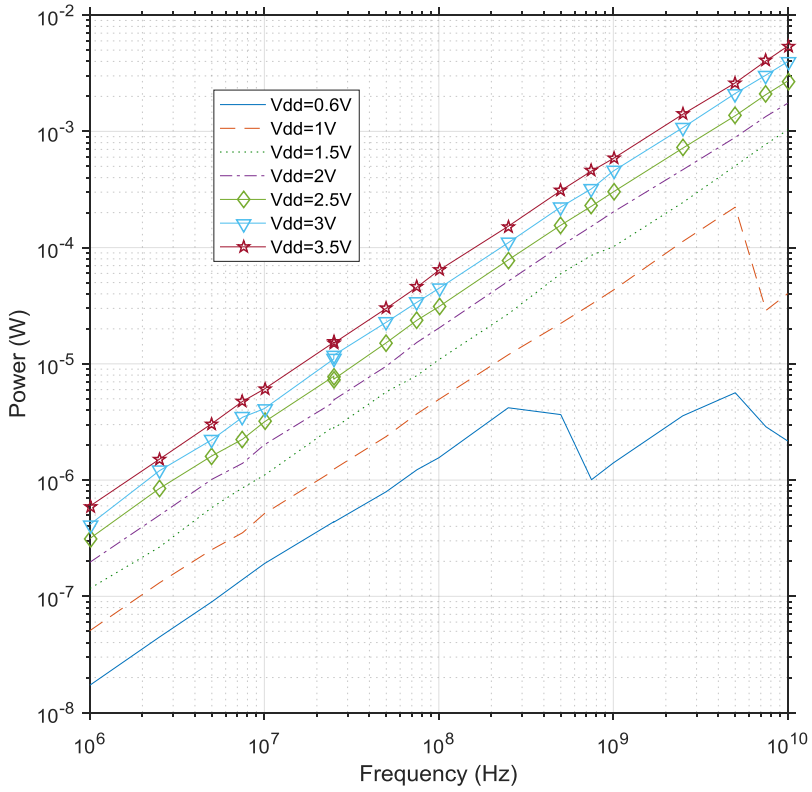


Figure (6.15): Power Consumption of a 22nm 16-Bit CRC Circuit.

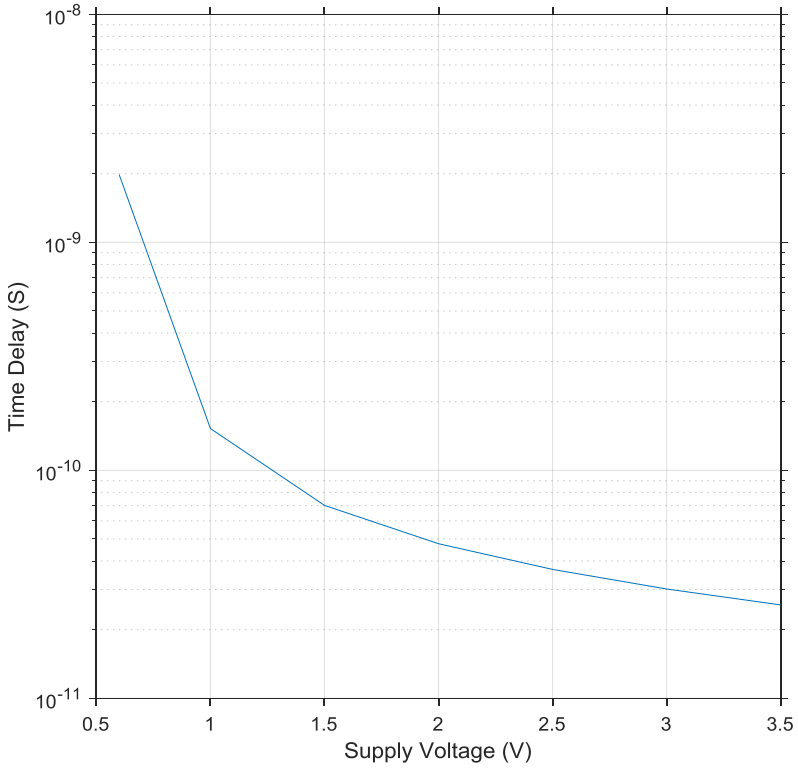


Figure (6.16): Time Delay of a 22nm 16-Bit CRC Circuit.

Again, the best technology size corresponding to power is the 22nm which is shown in the above figures. The power consumption of this circuit is higher than that of the 8-bit CRC because the number of gates in this circuit is higher than that of an 8-bit CRC circuit. SPM can make use of the time delay of the circuit to produce correct values of V_{dd} that reduce power and ensure an error-free operation of the circuit.

6.2.3. Limitation of the 24-Bit CRC Circuit.

Using the circuit described in section (5.3.3), the 24-bit CRC circuit was constructed using MATLAB. The circuit was tested under the same conditions of section (3.4), i.e. variable frequency variable V_{dd} for four technology sizes: 180, 90, 45 and 22 nm. The simulation results are shown in Figure (6.17) for the power consumption of the 180nm 24-bit CRC circuit while Figure (6.18) shows the time delay of the circuit. Figure (6.19) shows the power of the 24-bit CRC circuit of 90nm size, and Figure (6.20) shows the corresponding time delay. For the 45nm 24-bit CRC circuit, Figure (6.21) shows the power consumption and Figure (6.22) shows the time delay. Power consumption and time delay of the 22nm 24-bit CRC Circuit are presented in figures (5.23) and (5.24) respectively.

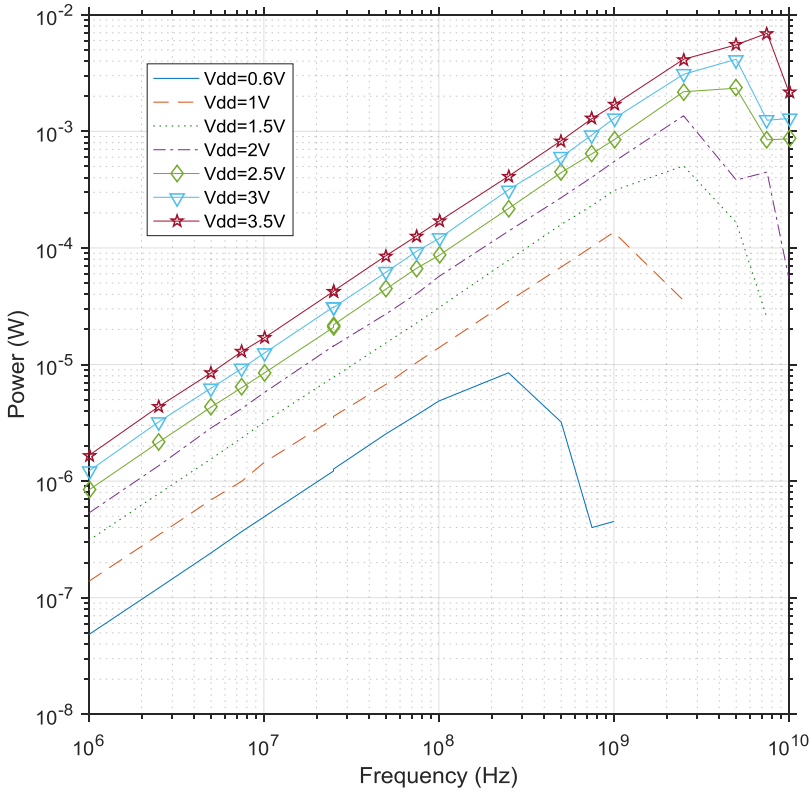


Figure (6.17): Power Consumption of an 180nm 24-Bit CRC Circuit.

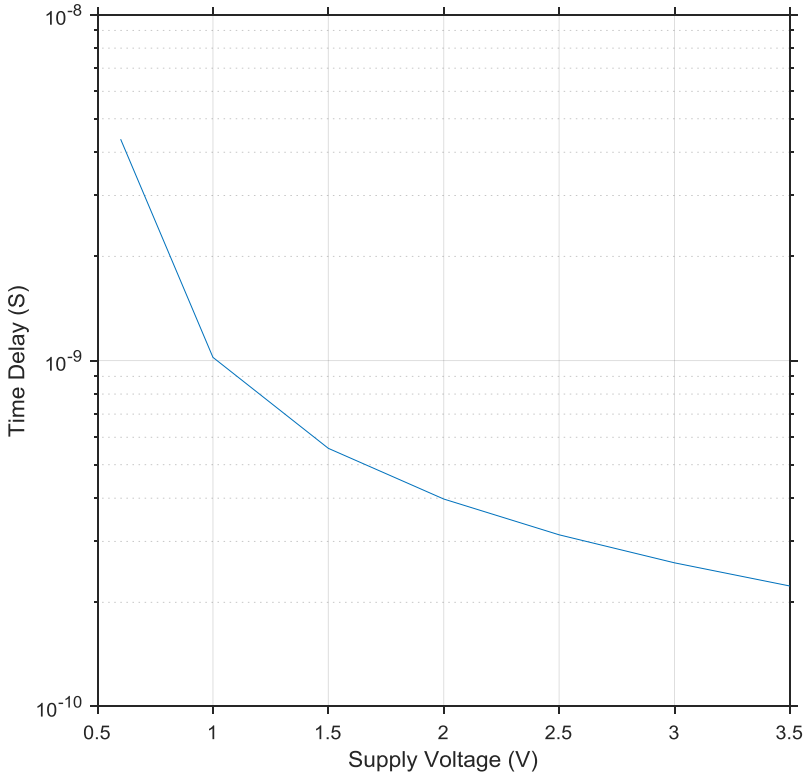


Figure (6.18): Time Delay of an 180nm 24-Bit CRC Circuit.

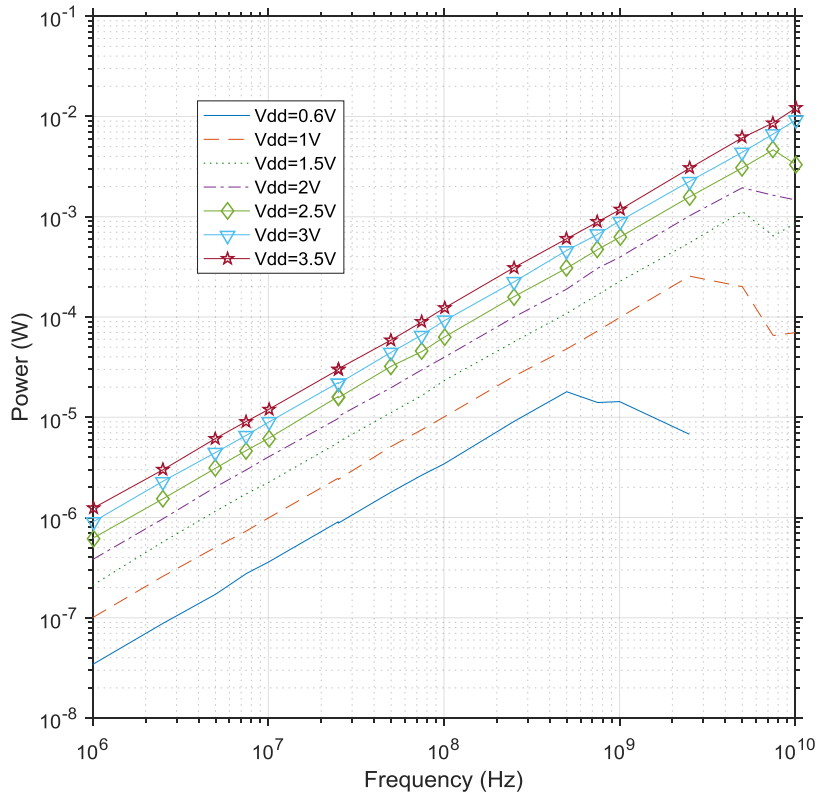


Figure (6.19): Power Consumption of a 90nm 24-Bit CRC Circuit.

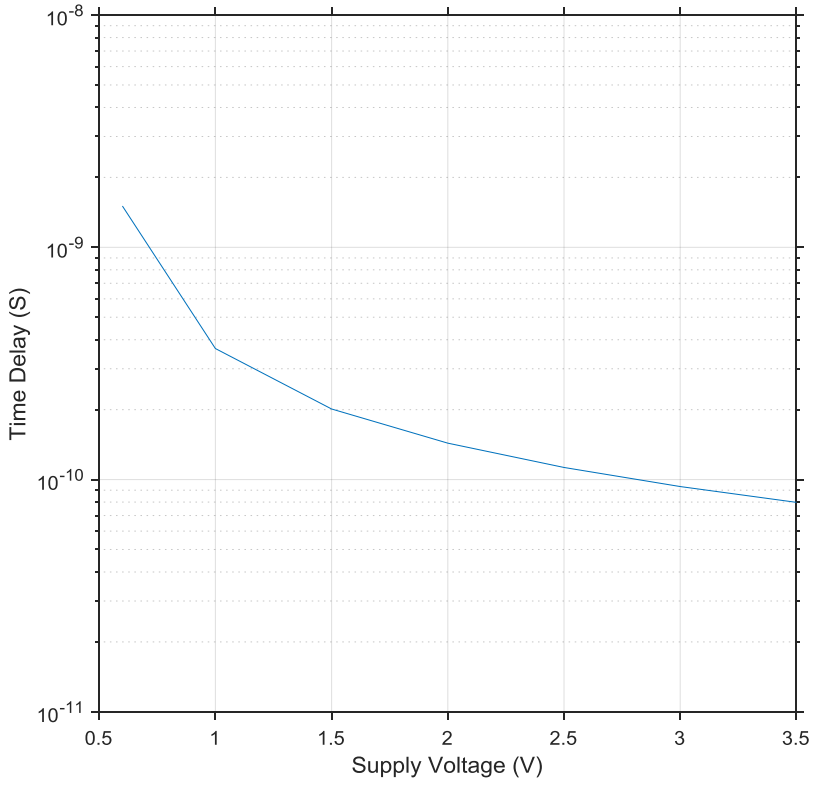


Figure (6.20): Time Delay of a 90nm 24-Bit CRC Circuit.

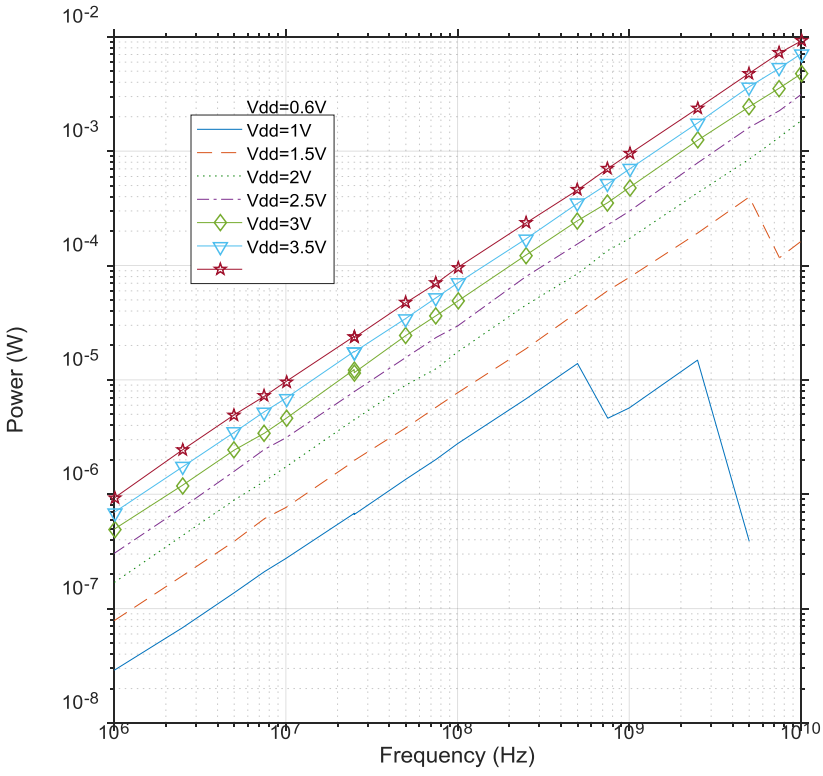


Figure (6.21): Power Consumption of a 45nm 24-Bit CRC Circuit.

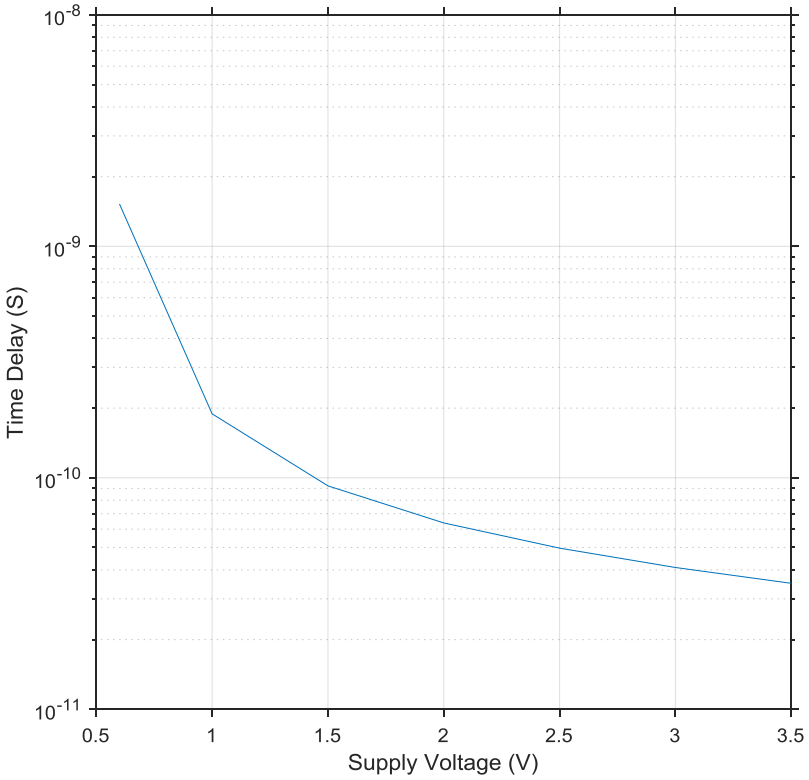


Figure (6.22): Time Delay of a 45nm 24-Bit CRC Circuit.

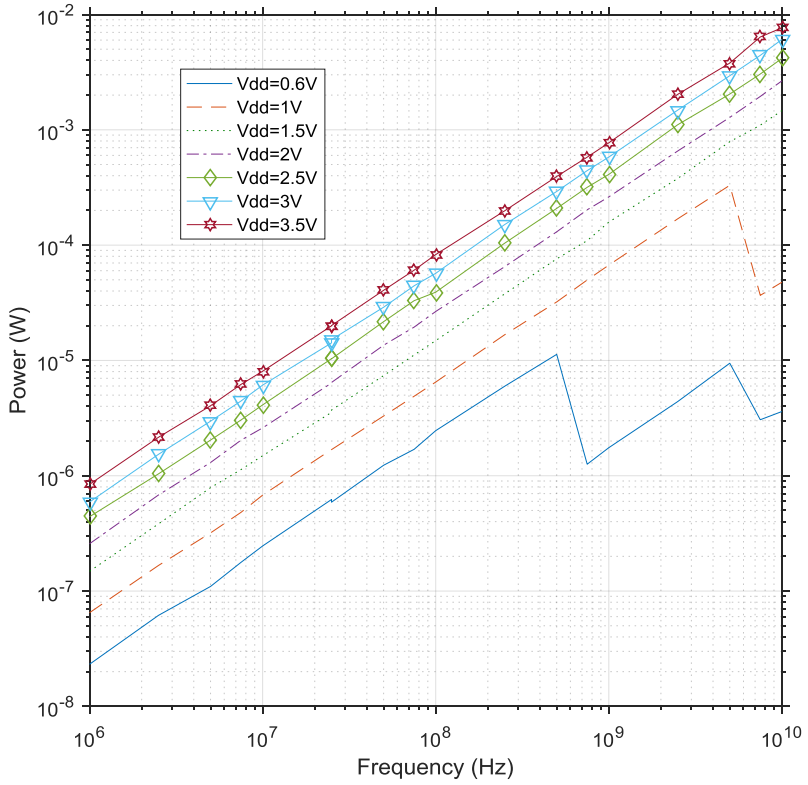


Figure (6.23): Power Consumption of a 22nm 24-Bit CRC Circuit.

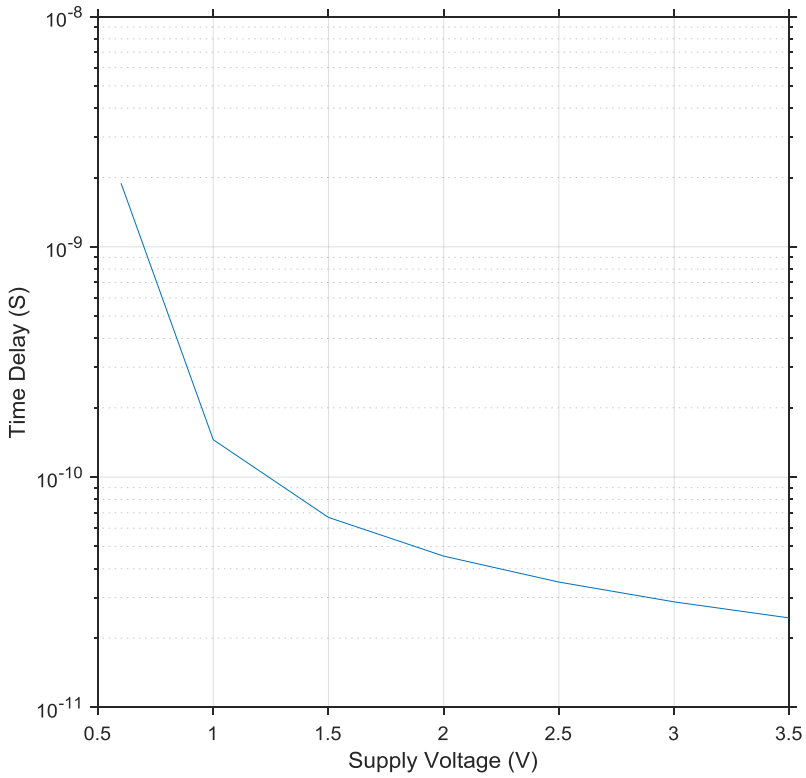


Figure (6.24): Time Delay of a 22nm 24-Bit CRC Circuit.

The circuit power of the 24-bit CRC is very close to that of a 16-bit CRC circuit because they have a close number of gates. Again, the time delay graph will provide the T_{max} value so that the course controller can decide whether to use the FLC V_{dd}, or use the maximum supply voltage. This feature will ensure an error-free operation of the circuit. T_{max} value of the circuit was calculated using equation (3.17) in section (3.3.1).

6.3. IMPLEMENTING THE SPM ON THE CRC CIRCUITS.

Using the SPM unit discussed in section (4.4), and the CRC circuits discussed in section (5.3), a simulation using MATLAB was made with 8, 16, and 24-bit CRC based on 22nm technology. Different frequencies were chosen as an input to the system to demonstrate the ability of the controller to deal with different conditions. The frequencies where chosen randomly for 10 intervals each of 1000 samples. The frequency set was [3.5MHz 27MHz 130MHz 750MHz 13MHz 2.5GHz 7MHz 300MHz 650MHz 80MHz]. The new SPM unit is shown in Figure (6.25). The results of the simulation were compared to another simulation of

the same system but with constant V_{dd} of 3.5V to show the ability of SPM to reduce power in different frequencies.

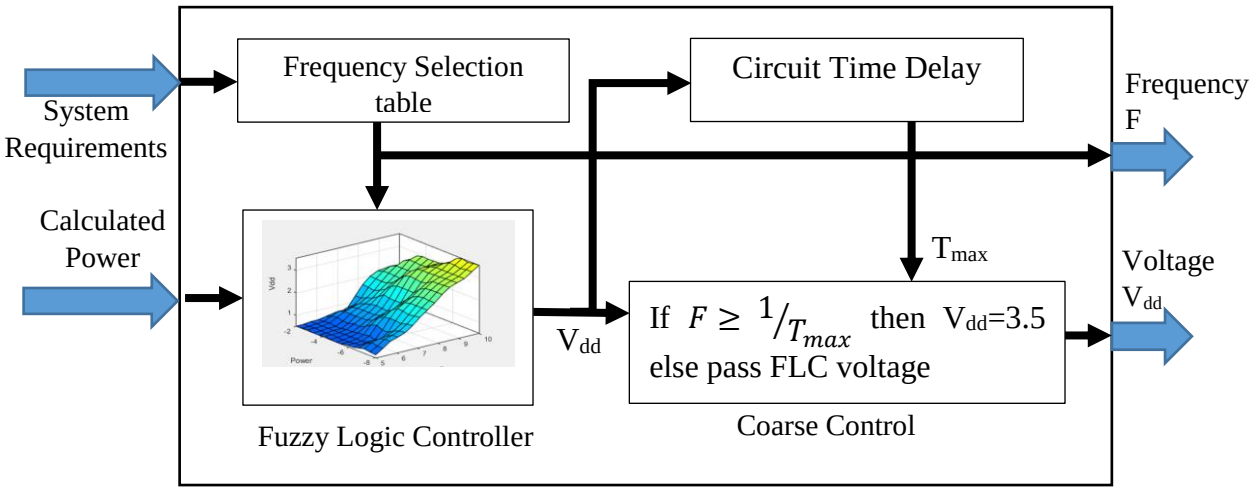


Figure (6.25): The Used SPM Unit.

The results of the simulation are shown below.

6.3.1. Reducing the 8-Bit CRC Circuit Power.

Applying the SPM unit on the 8-bit CRC circuit discussed in section (5.3.1) gives the power consumption of Figure (6.26). The supplied voltage from the SPM unit is shown in Figure (6.27). The delay time of the 8-Bit CRC circuit due to supply voltage change is presented in Figure (6.28). The percentage reduction in power due to the use of SPM is shown in Figure (6.29). These figures show the power consumed by the CRC8 only and it does not reflect how much power was consumed inside the SPM unite. It was shown in the literature that power manging circuits like the SPM can consume no more than 18% of the overall power (H. R. Pourshaghaghi & de Gyvez, 2010; Hamid Reza Pourshaghaghi & de Gyvez, 2009). To include the SPM power in this analysis, this figure should be conceded.

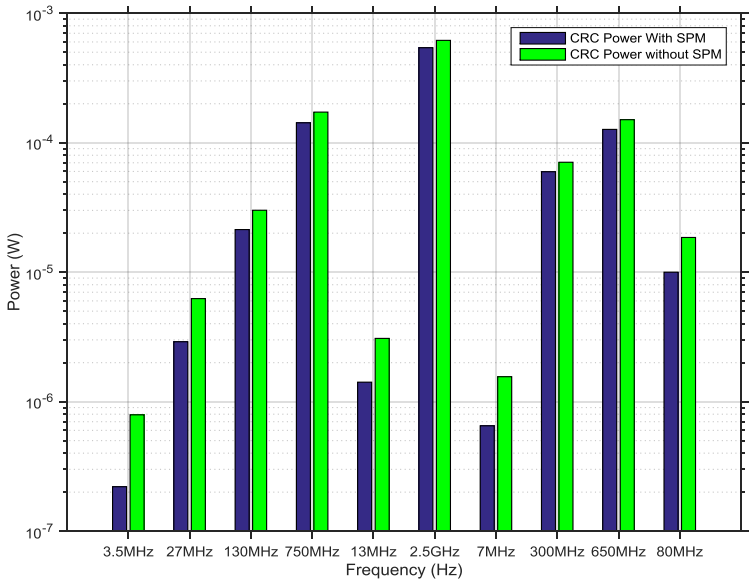


Figure (6.26): Power of the 8-Bit CRC with and without SPM.

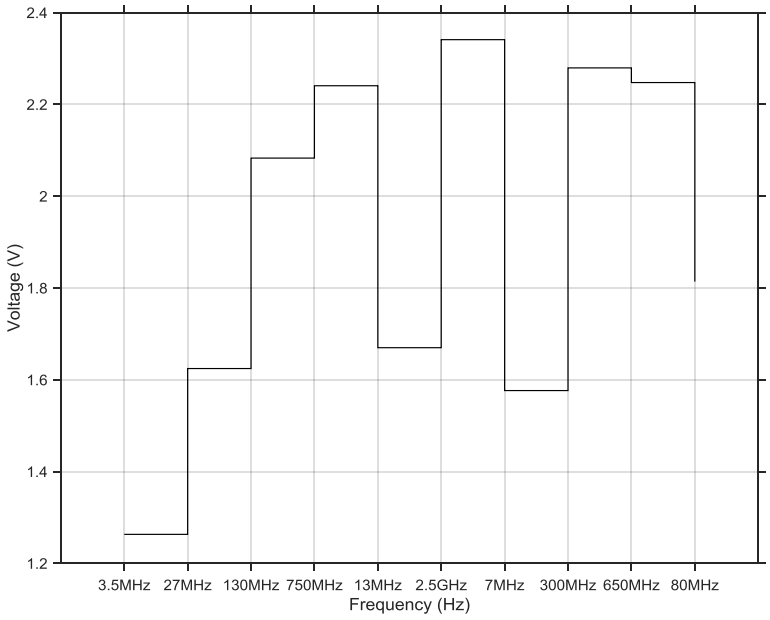


Figure (6.27): The 8-Bit CRC Controlled Voltage.

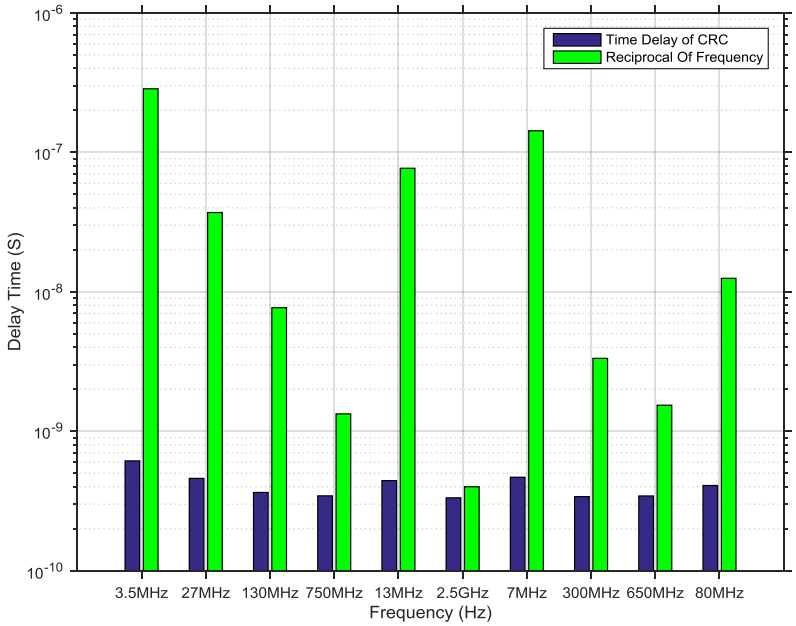


Figure (6.28): Time Delay of the Controlled 8-Bit CRC.

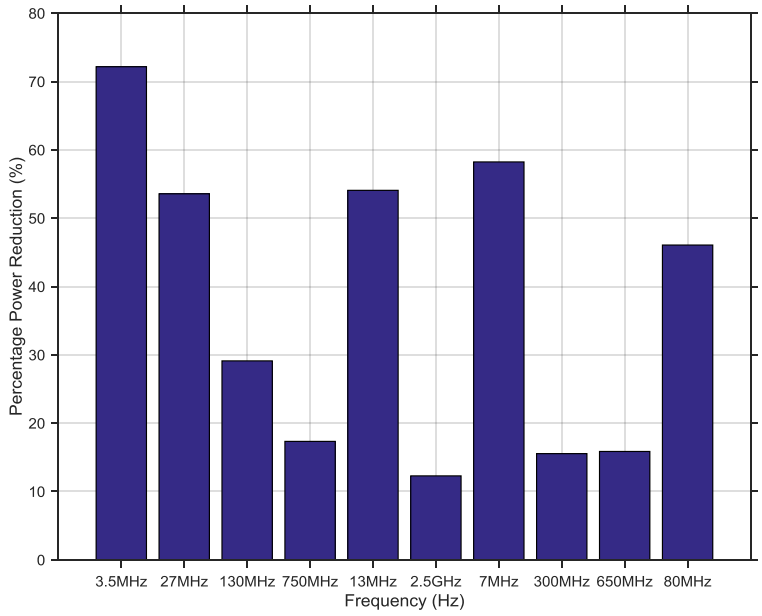


Figure (6.29): Percentage Reduction in the Controlled 8-Bit CRC Power.

The simulation clearly shows that SPM unit is capable of reducing the power of the 8-Bit CRC unit even when the frequency is high. The best performance is obtained in low frequencies that can reach up to 73% in the 3.5MHz, but it will decrease as the frequency

increases. At the 2.5GHz SPM managed to produce a power reduction of 12% and that makes it a good choice to reduce power in digital communication systems in different frequencies.

6.3.2. Reducing the 16-Bit CRC Circuit Power.

The 16-bit CRC circuit was simulated with the SPM unit. The power consumption of the circuit is shown in Figure (6.30). Figure (6.31) shows V_{dd} variation with the used frequency. The time delay of the circuit is presented in Figure (6.31), finally, Figure (6.32) shows the percentage reduction in power due to SPM.

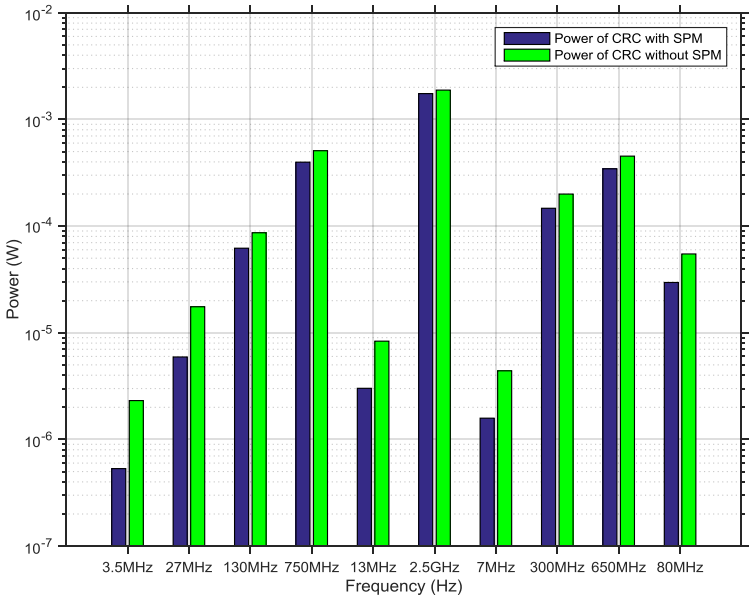


Figure (6.30): Power of the 16-Bit CRC with and without SPM.

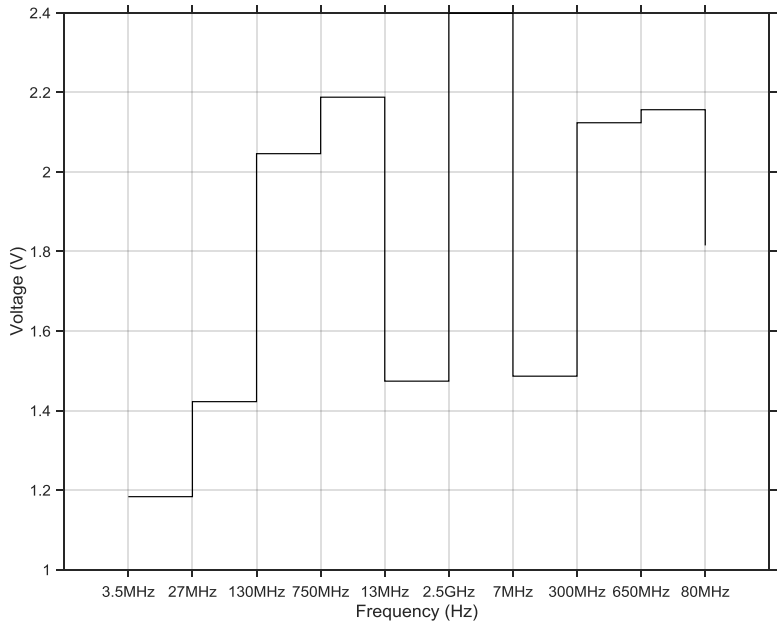


Figure (6.31): The 16-Bit CRC Controlled Voltage.

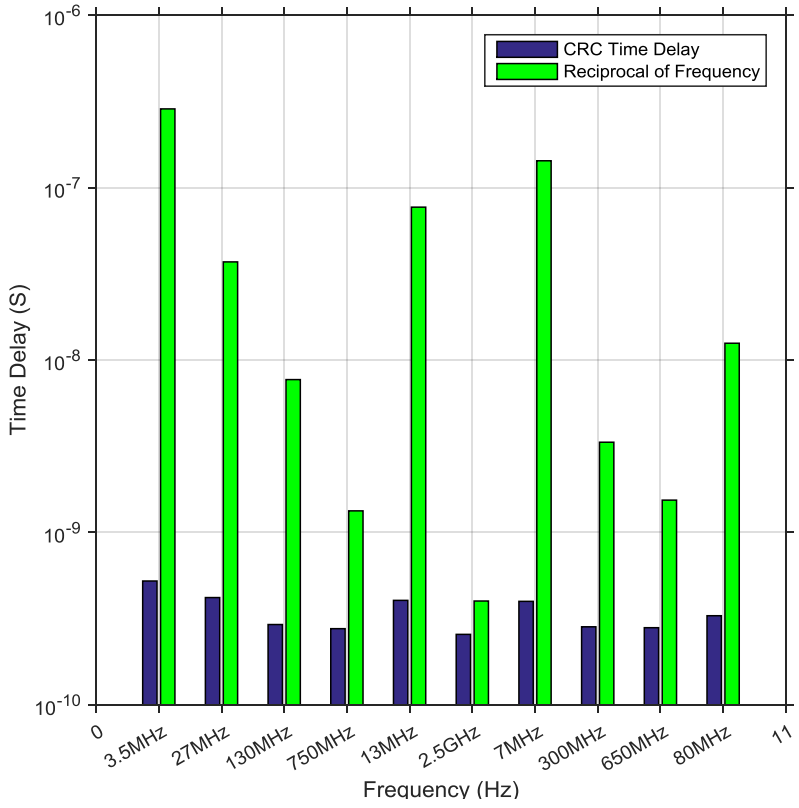


Figure (6.32): Time Delay of the Controlled 16-Bit CRC.

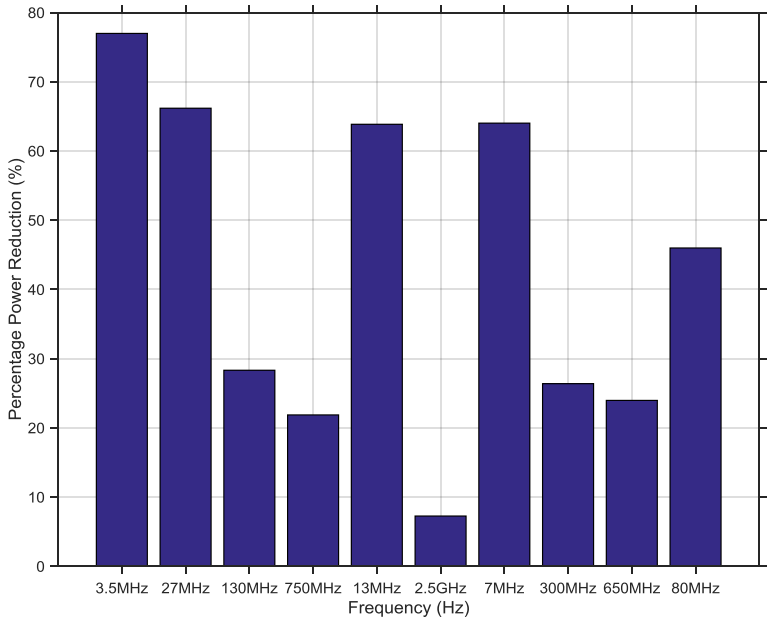


Figure (6.33): Percentage Reduction in the Controlled 16-Bit CRC Power.

Figure (6.30) shows that SPM was able to reduce the power in all cases even when the frequency is very high. The results of Figure (6.30) are supported by Figure (6.33), which shows clearly that the percentage reduction of power can be very high in low frequency. In very high frequency, the reduction is about 9%. A very important feature that can be seen from Figure (6.33) is that if the system is working under the same condition of Table (5.3), then there is a good chance that a power reduction of no less than 25% is achieved.

6.3.3. Reducing the 24-Bit CRC Circuit Power.

Applying the SPM unit on the 24-bit CRC circuit discussed in section (5.3.3) gives power consumption of Figure (6.34). The supplied voltage from the SPM unit is shown in Figure (6.35). The delay time of the 24-Bit CRC circuit due to supply voltage change is shown in Figure (6.36). The percentage reduction in power due to the use of SPM is shown in Figure (6.37).

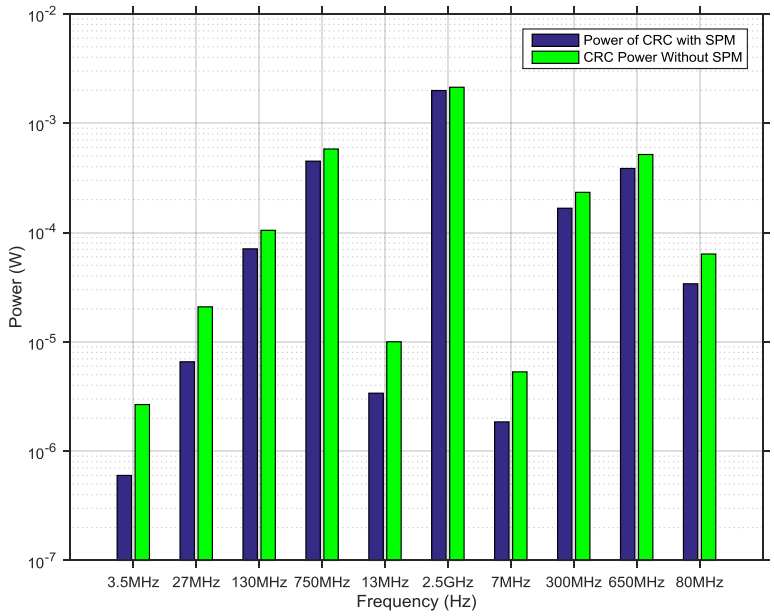


Figure (6.34): Power of the 24-Bit CRC with and without SPM.

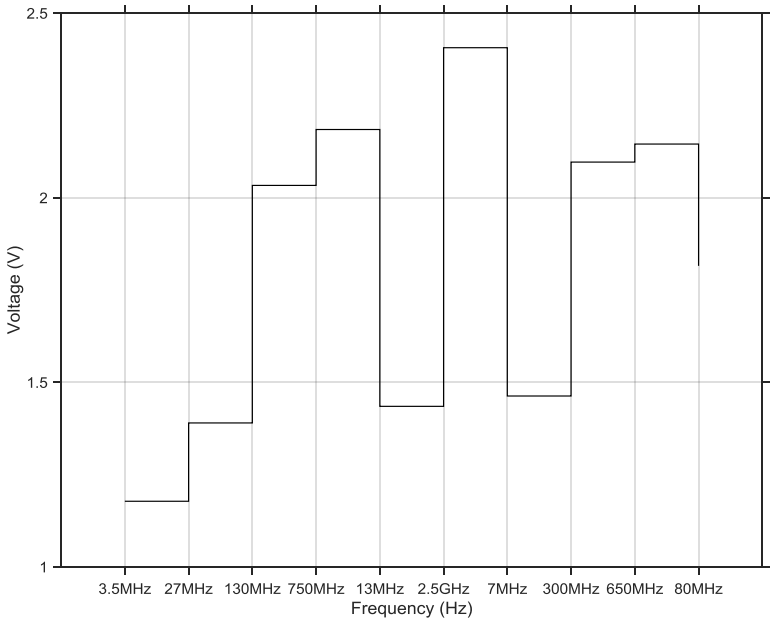


Figure (6.35): The 24-Bit CRC Controlled Voltage.

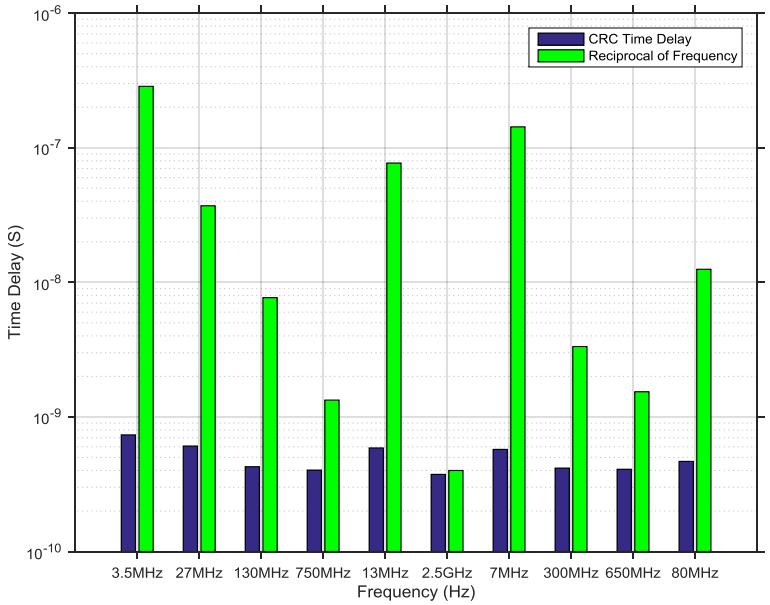


Figure (6.36): Time Delay of the Controlled 24-Bit CRC.

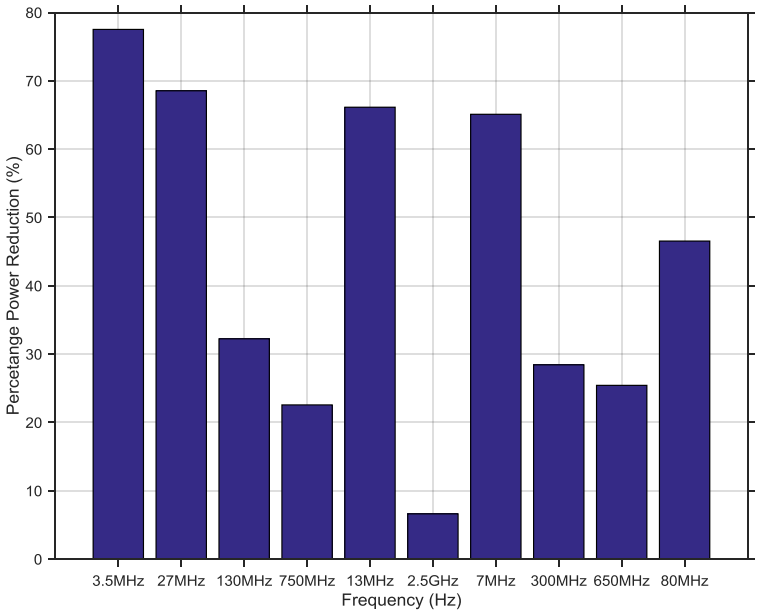


Figure (6.37): Percentage Reduction in the Controlled 24-Bit CRC Power.

The ability of SPM to reduce power is evident in this simulation. It managed to reduce power in 8, 16, and 24 bit CRC circuits. Although these circuits have the same functionality, they have a different architecture, different number of gates and different number of inputs. In all the cases, SPM was able to reduce the power even in high frequencies like 2.5GHz. It can reduce the power to 7% in this frequency for the 24-bit CRC circuit. Concurrently, the time

delay shows that SPM managed to keep the system time delay below the reciprocal of the frequency so that it can overcome the miss pulse error. The reduction of power in the range of 100-300 MHz is about 15-30%. This is a typical range for the operation of the CRC circuit.

6.4. CONCLUSION.

In this Chapter, a special block is added to a CRC stage to minimize the consumed power. The fuzzy logic controller was introduced as a controller in SPM and it was connected to the system and tested. The results show that SPM is capable of achieving a 75% in the MHz region and the power is controlled as the frequency increases. In the region of the GHz, SPM was able to reduce up to 7% of the consumed power because of the need for high voltage as a supply for the CRC circuit due to the miss pulse condition.

In the previous chapters, a new model of power in digital system was introduced. The model was used to assist building SPM that can control digital communication stages. CRC circuits were designed so that it could be used as a test bench for the SPM. In this chapter, these tests show the ability of SPM to reduce the consumed power of the circuits and maintain the system error free by monitoring the time delay of the circuit so that the best supply voltage is chosen for the circuit. In the next chapter, SPM is introduced to the LTE system so that a special controller unit is built to generate the required V_{dd} and frequency for the LTE stages. The voltage and frequency pairs will ensure power reduction according to the used modulation technique.

CHAPTER SEVEN

THE SPM FOR LTE COMMUNICATION SYSTEM: A CASE STUDY

7.1. INTRODUCTION.

Long Term Evolution (LTE) is the key technique that defines 4G communication systems. Its unique capability of occupying the channel capacity and its use of the Orthogonal Frequency Division Multiplexing (OFDM) access enable it to achieve very high data rates in its output (Cox, 2012). This high bit rate is possible because LTE uses different encoding techniques to reduce its Bit Error Rate (BER), as well as different modulation techniques to take full advantage of its allowed spectrum (3GPP Specifications, 2015b, 2015c; Penttinen, 2011).

In this thesis, SPM was built to reduce the power of a communication system. In the previous chapter, SPM was implemented successfully in a communication system and was able to reduce the power depending on the input frequency. SPM managed to keep the system error free although its task was to reduce V_{dd}. In this chapter, a case study is made to implement SPM in LTE communication system. SPM will make use of the diversity of techniques used in LTE to reduce the power according to the used modulation and CRC techniques.

7.2. DESCRIPTION OF THE LTE SYSTEM.

The modulation techniques used in LTE are 16 and 64 Quadrature Amplitude Modulation (QAM), as well as Quadrature Phased Shift Keying (QPSK). While in its coding part, it uses 8, 16, 24A and 24B CRC in addition to Turbo codes to improve its SNR (3GPP Specifications, 2015c; GPP, 2012). To maintain a constant throughput, LTE architecture should use two mechanisms that govern the data rate between different stages of the system. The first is to use buffers between the stages so that it matches the throughput between them. The second method is to use different clocks to govern the stages so that the bit rate is constant along the data path (Stallings, 2013). In this case study, the second mechanism is used so that different frequencies were taken as the stages clocks. The reason behind this selection is to make use of the clock frequency difference between stages so that SPM can reduce power. These frequencies were utilised to work out the best voltage for the CRC. The frequency and voltage pair should ensure less power consumption from the CRC stage. The voltage and the system frequency are supplied from the SPM unit that takes the system requirements as its input. Letting the SPM decide the system clock frequency will reduce the overhead from the GPP and give SPM full control on the digital communication system.

Since the CRC techniques are used in different channels rather than the same channel, and since the modulation techniques are associated with these channels, then the system will

assume that it may use any CRC with any modulation technique at any time. This feature will enable the CRC stage to work in the uplink and downlink of the system which will reduce the number of used circuits and the area.

The CRC circuit discussed in section (5.4) is used alongside the modulation stage. The SPM unit generates the required frequency and voltage to the CRC so that the dynamic power of the stage is reduced.

7.2.1. Clock Setting of the LTE Units

In this section, the clock frequency needed to control the data transfer between stages is discussed. These frequencies are stored in a table inside SPM so that it can predict the needed clock frequency by the type of the modulation and CRC used. At the same time, SPM will calculate the voltage associated with these frequencies and supply the stages with it.

A look at the LTE system specifications is required to calculate the clock frequency of the CRC stage. According to (3GPP Specifications, 2015a, 2015b; Cox, 2012; Penttinen, 2011), the Fast Fourier Transform (FFT) of the OFDM stage requires 2048 FFT points and a sampling time (T_s) of 32.55 ns to produce its output. This number comes from the fact that this stage takes 2048 FFT points for each carrier. The carrier frequency is 15 kHz. Hence, the data rate needed as an input to this stage is equal to k×30.72 Mbps. k is the number of bits per FFT point.

Assuming that the modulation stage is producing k output bits per input sample, the frequency needed at this stage is 30.72 MHz.

To produce its output, QPSK, the 16 and 64 QAM requires 2, 4, and 6 bits as input. Hence, the input data rate of this stage should satisfy the throughput requirements of the output. This implies that if the 64 QAM modulation was used, then the data rate should be 6 bits × 30.72 MHz, which in turn gives 184.32Mbps. The bit rate corresponding to each modulation technique is given in Table (7.1). These figures make calculating the needed clock frequency for the CRC stages possible.

Table 7.1: Bit Rates for Different Modulation Techniques in LTE

Modulation Technique	QPSK	16QAM	64QAM
Data Rate (Mbps)	61.44	122.88	184.32

For simplicity sake, assume that the CRC stage is directly connected to the modulation stage and there is no need for the turbo encoder stage.

The CRC stage produces 8, 16, or 24 bits depending on the coding scheme that may be used. The frequency governing this stage can be calculated from the number of bits produced by the CRC stage and the throughput required by the modulation stage. For example, a 16 bit CRC and 16 QAM combination should generate a clock frequency of 122.8Mbps/16bit which equals 7.68MHz. Therefore, based on the previous discussion, the clock frequency that governs the CRC stage should be as in Table (7.2).

Table 7.2: CRC Stage Frequency According to the Number of Bits and the Used Modulation.

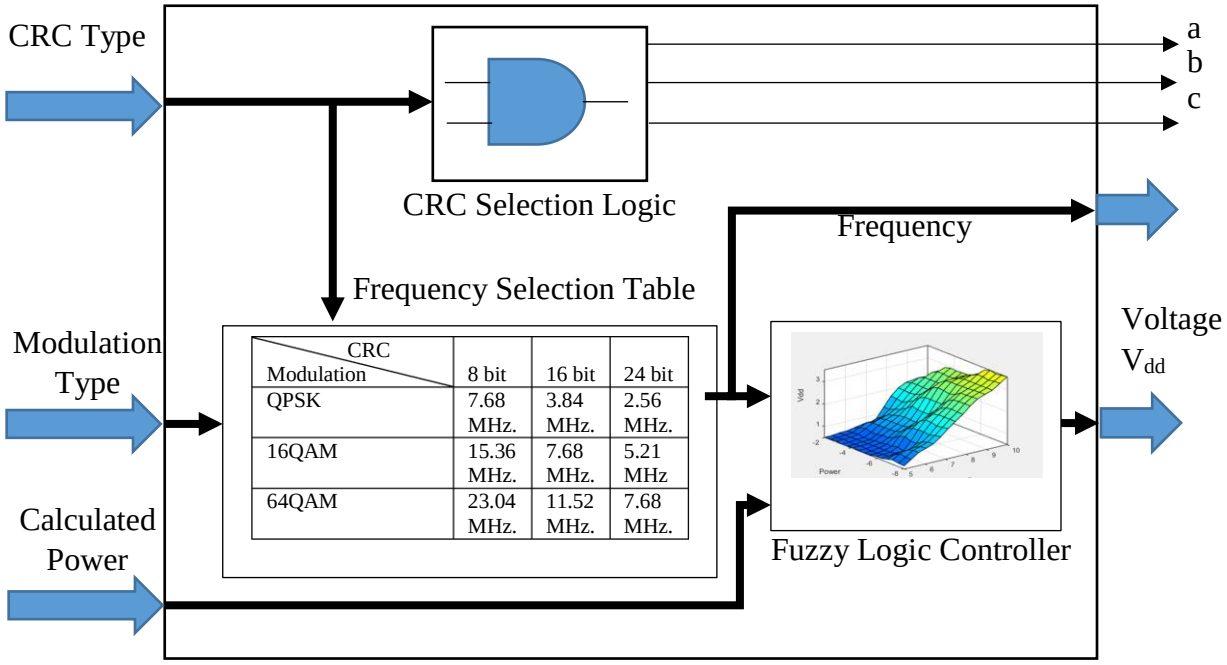
CRC Modulation	8 bit	16 bit	24 bit
QPSK	7.68 MHz.	3.84 MHz.	2.56 MHz.
16QAM	15.36 MHz.	7.68 MHz.	5.21 MHz
64QAM	23.04 MHz.	11.52 MHz.	7.68 MHz.

According to the used CRC and modulation technique, SPM relies on the figures presented in Table (7.2) to decide the best frequency to be used by the CRC stage. Therefore, if a 16QAM modulation technique is needed with 16 bit CRC, then the required frequency to the CRC stage is 7.68 MHz. This clock frequency ensures that the bit rate supplied by the CRC stage will not conflict with the bit rate needed for the input of the modulation stage.

7.3. DESIGN OF SPM FOR LTE.

To control the LTE CRC unit, the same SPM design of section (6.3) was used but with modification to the unit. The design is shown in Figure (7.1). The inputs to the unit are the CRC type, Modulation type and measured CRC power. The CRC and modulation type represent the system requirements.

The system requirements will determine the needed clock frequency to the CRC unit inside the frequency selection table. The clock frequency is fed into the FLC that will produce the required V_{dd} to the CRC stage according to the fuzzy surface shown in Figure (4.3). The CRC selection logic is a 2×4 DeMUX circuit that will choose the required CRC circuit by asserting the required selection line (a, b, or c). The outputs of SPM are three CRC selection lines, CRC clock frequency, and CRC supply voltage.



CRC / Modulation	8 bit	16 bit	24 bit
QPSK	7.68 MHz.	3.84 MHz.	2.56 MHz.
16QAM	15.36 MHz.	7.68 MHz.	5.21 MHz
64QAM	23.04 MHz.	11.52 MHz.	7.68 MHz.

Figure (7.1): SPM unit for the CRC Power Control in LTE System.

7.4. IMPLEMENTATION AND RESULTS.

To control the power of the CRC circuit, SPM was designed according to the description given in section (7.3). By using 22nm CMOS technology and the multi polynomial algorithm, the CRC of section (5.5.2) was implemented using MATLAB. The circuit can perform the operation of the 8, 16, and 24 bits CRC polynomials. Three types of modulations were used with each CRC polynomial, namely: QPSK, 16QAM, and 64QAM. Thus, nine frequencies were applied to the system according to Table (7.2). These frequencies ensure a constant bit rate at the output of the stage.

The SPM will supply the voltage of the system before the start of operation and keep it fixed until the next system change. When the system change, SPM will make use of the calculated average power and the new system requirement to produce the new supply voltage to the CRC stage. The calculated average power is calculated using the new power model algorithm discussed in section (3.3.2).

The simulation started by assuming a fixed 1000 block of data supplied to the CRC stage for each interval. The block of data has the same number of bits of that of the CRC stage, so if a CRC8 was used then the system was fed by 1000 block of 8 bit data, if CRC 24 is used then the system was fed by 1000×24 bit block.

The system was compared to a multi-polynomial CRC with a fixed voltage supply of 1.8 volts and a clock frequency of 30MHz. Figure (7.2) shows the consumed dynamic power of the two systems, while Figure (7.3) shows the averaged supplied voltage from the SPM stage. Figure (7.4) represents the percentage reduction in the system power due to the use of SPM compared to the fixed voltage and frequency system.

Another setup was made to compare the system with the proposed SPM, with a CRC system that has a fixed 1.8 volt and variable frequencies that are taken from Table (7.2). The resulting average power is shown in Fig. (7.5) while the percentage reduction of power is shown in Fig. (7.6).

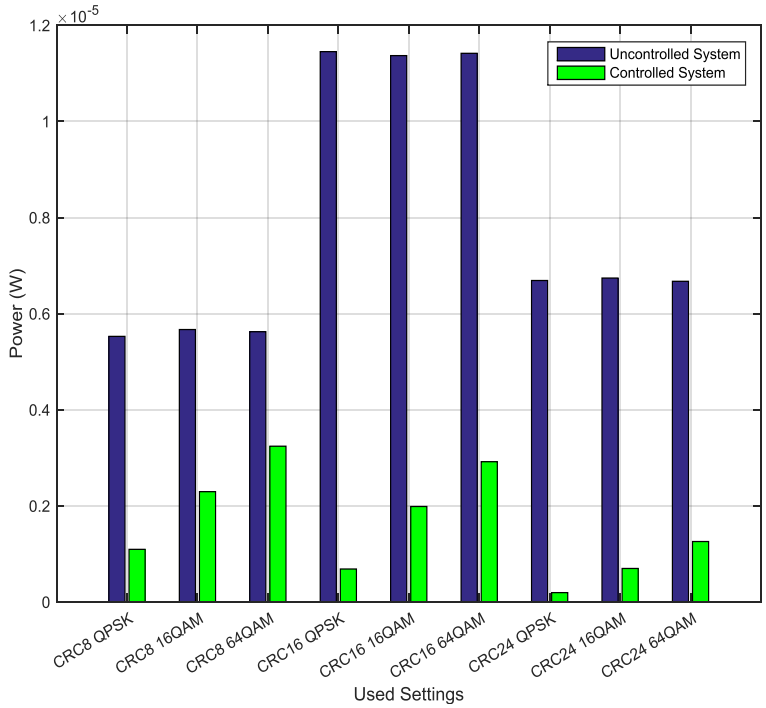


Figure (7.2): Comparison of Power Consumption of the CRC stage Between the Fixed Frequency System and SPM for Different Modulation Techniques.

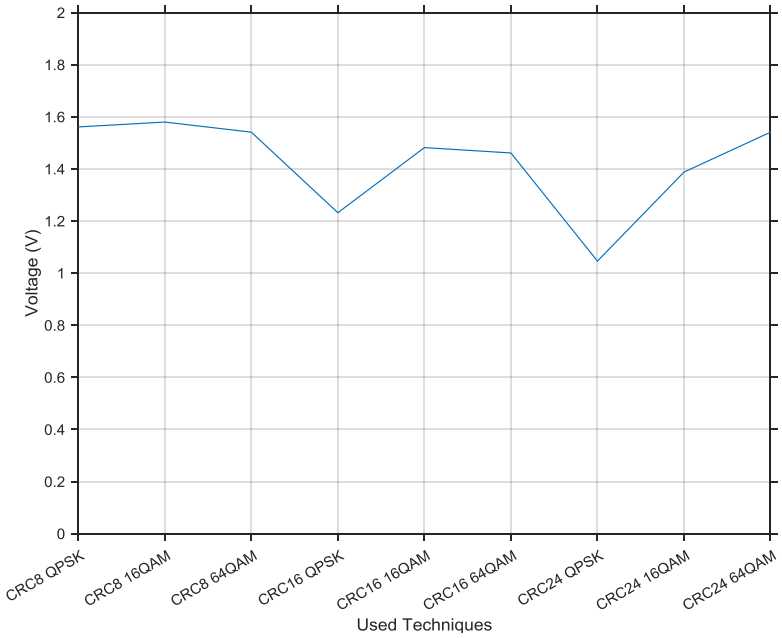


Figure (7.3): The Voltage Supplied by the SPM.

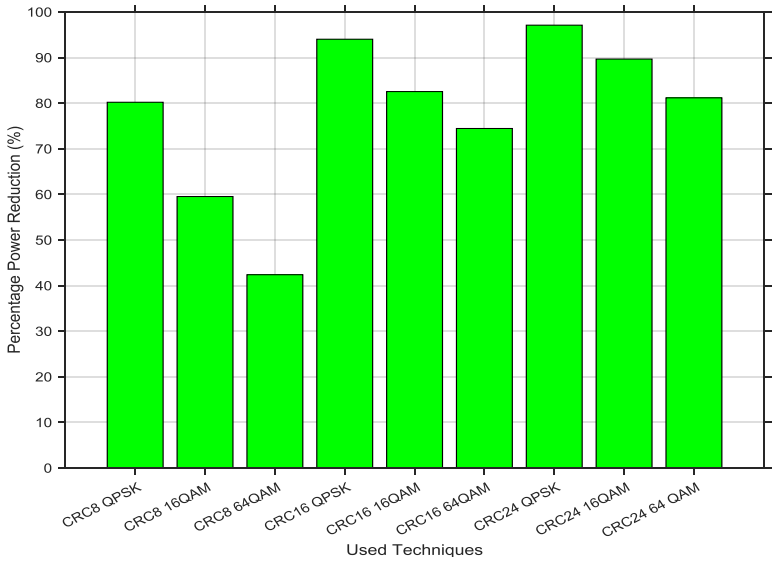


Figure (7.4): Percentage reduction in Dynamic power due to the use of SPM for the First Setup.

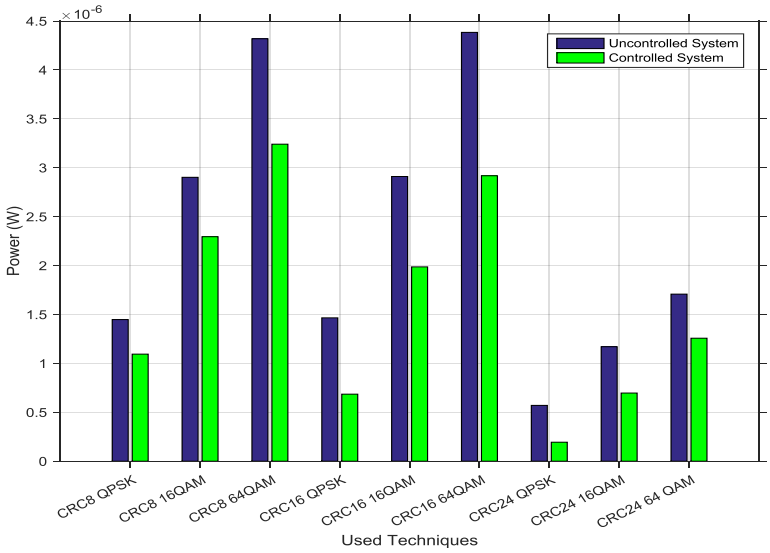


Figure (7.5): Comparison of Power Consumption of the CRC stage Between the Variable Frequency System and SPM for Different Modulation Techniques.

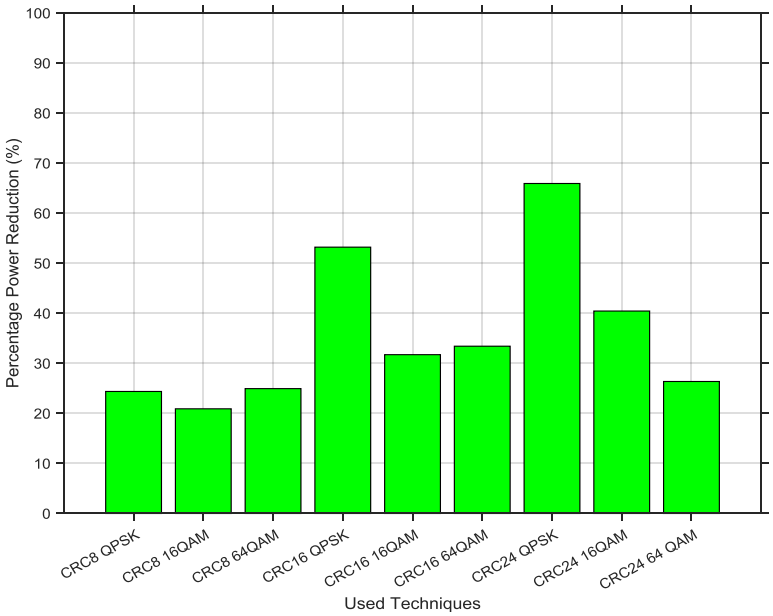


Figure (7.6): Percentage reduction in Dynamic power due to the use of SPM for the Second Setup.

7.5. CONCLUSION.

In this Chapter, an SPM was designed to control the power of a CRC stage for the LTE system. The CRC stage is capable of encoding the data according to g_{CRC8}, g_{CRC16}, and g_{CRC24b}. The SPM stage produced the clock frequency according to the needed modulation and encoding type. The CRC supply voltage stage is calculated by the SPM stage using a fuzzy logic controller to reduce the power of the system. The supplied voltage will not affect the system throughput. It should be noted that the power consumed in the SPM unit was not included in

the results. From Figure (7.2) it is clear that the dynamic power dissipation of the controlled system (with SPM) is less than that of the fixed frequency system. Furthermore, the use of SPM reduced the consumed dynamic power of the system compared to a system that uses different frequencies, which is evident from Figure (7.5). The percentage of reduction in dynamic power in the first case is more than 40 %, and it can reach up to 97% (Figure 7.4). In the second case, Figurs (7.6) indicates that the percentage reduction lays between 21%-66%. Figure (7.3) shows that SPM can change the supplied voltage according to the needs of the system. The voltage will increase when a higher frequency is required, but at the same time, this growth of voltage will not lead to a higher power consumption. Further investigation into Figures (7.2) and (7.5) shows that the use of the constant frequency without SPM, will keep the power consumption in one level for each CRC used (0.055 μW for CRC 8, 0.11 μW for CRC 16, and 0.068 μW for CRC 24), while using different frequencies for the system can enhance the power consumption of the system as it was shown in Figure (7.5). This proves that the use of the frequency as a controlling parameter will ensure a significant reduction in power consumption of the digital circuit. Another important feature that could be seen from Figure (7.5) is that the change in frequency was implemented to ensure a constant data rate between the transceiver stages, which was utilized to reduce more power especially in CRC 24. It could be seen from Figure (7.2) that the power consumed in CRC24 is bigger than that of the CRC8, while in figure (7.5) the power dropped significantly due to the proper use of the frequency.

From the above discussion, it is clear that the use of frequency as a control parameter can enhance the dynamic power reduction in digital communication circuits. Furthermore, the use of SPM in such circuits will reduce power consumption. This reduction is possible since SPM selects the optimal voltage for the circuit. The voltage will ensure that the system is far from producing errors, and at the same time, consumes less power.

CHAPTER EIGHT

CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

8.1. SUMMARY.

In this thesis, the aim was to reduce power in communication systems, especially in mobile devices. The research started by investigating the types of multi standard digital communication systems. The aim of this investigation was to select the best suited system so as to be the norm of the thesis investigation. The PRFP was the target of this investigation since it used well-defined communication units. Its power consumption was low, and it was adaptable and reconfigurable so that it could work with different communication standards.

The second step after choosing the target communication system was to investigate how power is consumed in digital circuits in order to identify the parameters that affect power consumption in the digital circuits. These parameters can give a better understanding about how to reduce the consumed power in digital circuits.

The third step in this research was to look at the methods of power reduction in digital systems. The aim of this step is to select a method that can be used in the multi standard digital communication system. DVFS was chosen due to its ability to reduce the overall consumed power of the digital circuit by reducing the supply voltage. Another feature that makes this method the best choice among power reduction methods is its ease of implementation and control. Its only limitation in communication system is that it uses the task time as a governing parameter and that does not exist in communication circuits. This limitation was overcome by using the clock frequency of the system as the controlling parameter to this method.

From the energy equation of the CMOS circuits, a proposed model for power consumption in digital circuit was derived. This model includes the load capacitor of the gates, the effect of input changes on the gates, and connectivity of the gates. These parameters were not accounted for in the previous power models. To verify the integrity of the model, it was implemented using MATLAB to measure the power consumption of the NOT gate, 2×1 MUX, 1-bit FA, and 2-bit FA circuits. These are the most used circuits in digital systems. The results of the new power model were compared with an implementation to the same circuits using OrCAD Cadence. The simulation showed that the new power model can simulate the dynamic power consumption of the digital circuit efficiently. Furthermore, the new model can work with large digital systems which is a privilege OrCAD Cadence cannot provide.

In many SDR and multi-standard communication systems, clock frequency changes to cope with the changing requirements of the system. This feature is used in this research to build SPM. SPM is a smart unit that can make use of the frequency changes to manipulate the

supply voltage of the system so that it reduces the dynamic consumed power. SPM uses the clock frequency and the measured power as its input, and produces V_{dd} as the output. The core of the SPM is an FLC that has rules designed specially to reduce power without affecting the time delay of the logic circuit.

SPM was tested using 2×1 MUX, and 2-bit FA circuits. The test took place using different frequencies ranging from few MHz to GHz. The reason for this range is that for SDR the targeted operating frequency is very high. The high frequency range was chosen to prove the ability of SPM to fit in SDR. To deal with such a kind of range, a log scaling technique was used so as to map the frequencies and measured power into the corresponding fuzzy universe of discourse.

The results of the simulation showed that SPM can reduce power in all frequency ranges. It is most powerful in the low frequency ranges but it can reduce no less than 10% of the consumed power in very high frequencies.

The first stage of the Tang architecture was the CRC stage. This stage was explored to produce parallel circuits capable of producing the 8, 16, and 24 bit CRC remainder. These circuits are the norm of the LTE standard. To reduce the number of gates, the size, and hence the power of such circuits, a new multi-polynomial circuit was designed. This circuit combined the three CRC circuits into one general circuit that has a fewer number of gates and size. The multi-polynomial circuit can work under the LTE standard and produce the required remainder by selecting it using three selection lines.

The 8, 16, and 24 bit CRC circuits were used as a test bench for the SPM to prove the SPM ability to reduce the power in digital communication systems. The same frequency range was used in this test. The SPM proved its ability to control the consumed power efficiently even in very high frequency.

The SPM unit was tested using many circuits. Some of these circuits were very small in size and some were large. The circuits had different architectures, and number of inputs. In all the situations, SPM was able to reduce the circuit’s power using only the power readings and the clock frequency of the system.

The final step in this research was to implement SPM in an LTE system. The system clock setting was discussed to find the point in which the system clock frequency needs to change. The point was when changing between CRC circuits and the type of modulation. This point happened because the system needed a constant throughput at the output. SPM uses these

changes to efficiently reduce the consumed power in the CRC stage especially when a 24 bit CRC was used with the QPSK modulation.

8.2. CONCLUSIONS

In chapter one, a look at the used communication circuits was made. There are many systems capable of performing the required communication tasks, but the chosen system (PRFP) was able to adapt according to the needs of the used communication standard. The conclusions driven from this choice were:

- It is better to isolate the communication tasks rather than mixing them with other tasks in one chip. This will enable GPP to handle other non-communication applications efficiently.
- Separating the communication tasks will make it easier to analyse and calculate the amount of power wasted in each communication unit or task. This feature will give a better understanding of how power is consumed regarding the used communication method or technique.
- Reconfigurable communication hardware can cover a wide area of communication standard easily.
- If the coprocessor software and hardware are reconfigurable, then it is easier to implement new technology on such a device, leading to an increase in the adaptability of the system.

Reviewing the power reduction methods in digital systems showed that there are many levels in the design that can affect power consumption. It starts from the full system to the blocks of the system and ends with individual digital circuits. A look at these methods gave the following points

- Studying the power consumption in each level can reduce a significant amount of the consumed power of the system.
- Choosing a power reduction method must depend on the parameters that affect the power in the circuit, e.g. DVFS reduces Vdd to reduce the overall power.

- Understanding how each parameter in the power equations affect power consumption and the behaviour of the circuit or system will lead to building more robust power reduction methods.

Investigating the parameters that affect power consumption in digital circuits showed that the used power model did not account for all the variables that affect the consumption of power. Therefore, a new model was built. The conclusions driven from the new power model are:

- The new power model can predict the consumed power efficiently.
- The new model can show the frequency limits of the digital circuits, and hence, it can give a better estimation of its behaviour in a wide frequency range.
- The new model can easily show how much power is consumed in the glitches. This feature is not included in the previous power models.

SPM was designed in chapter four. It was tested using different digital circuits, and variable frequencies. The simulation shows the following points:

- The use of FLC in the circuit is a necessity since the circuit model is highly stochastic. Another point that made FLC as the best controller for this system is that it does not need a huge computation power and storage. This feature means that FLC consumes less power than other controllers working in the same field.
- From the FLC design, it was seen that if the input has a wide range, FLC could still work properly if the input was scaled using log scaling techniques.
- SPM was able to reduce the consumed power significantly in all of the frequency ranges.
- SPM can work at its best in low frequencies. Its efficiency is reduced in high frequencies since it tries to compensate for the circuit time delay. This means that it reduces the voltage to a certain level corresponding to the used clock frequency.

To implement SPM in communication circuits, the CRC stage was chosen as the target for power investigation. The process of designing this stage showed that:

- Using unfolding technique can significantly reduce the clock frequency leading to the reduction of the consumed power.
- The state space and unfolding techniques can work with any CRC generator.

- It is possible to combine many CRC circuits into one circuit by using the multi-polynomial algorithm discussed in chapter five.
- The new multi polynomial circuit has a fewer number of gates, lower size and lower power consumption than the ordinary CRC circuits.

Using SPM on the CRC circuits showed that:

- SPM can work with large circuits like the 24 bit CRC circuit.
- SPM can reduce the power of the circuit efficiently even in high frequencies.
- SPM managed to work with different circuit that are all used in digital communication. It makes it a good choice as a power managing technique in digital communication systems.
- To design a good SDR system, the components need to work in very high frequencies. Since SPM proved its ability to work under the same conditions, it can be used to reduce power in SDR systems.

The final setup was to use SPM in an LTE system. The setup investigated the use of the multi-polynomial CRC circuit with different modulation techniques. The outcomes of this study are:

- The SPM made use of the clock frequency variations in LTE to reduce the stage power.
- There are other places in LTE that have this diversity in the clock frequency which makes it possible to reduce more power in LTE system.
- SPM proved its ability to reduce power specially when the used CRC is the 24 bit CRC and the modulation is the QPSK.
- Reducing the number of constellation in the modulation stage will reduce the consumed power due to the need for a smaller clock frequency.
- Increasing the number of CRC bits will decrease the used clock frequency which leads to a lower power consumption.

8.3. SUGGESTIONS FOR FUTURE WORK

The following points should be considered for future work:

- The new power model did not account for the heat model of the CMOS chips. This model will limit the use of the supply voltage. Including the parameters that affect this behaviour will produce a more accurate power model to determine the full range of the voltage. This will lead to a better understanding to the used voltage range in digital circuits.
- A new trend in CRC circuit is called the CRC on-the-fly. It can reduce the latency time of the reminder calculation by reducing the data width while in operation (Weithoffer & Wehn, 2015). Applying this method of CRC calculation with the multi-polynomial CRC is a challenging task, and it can produce a powerful circuit that can consume less power by reducing the number of gates, and in the same time reduce the latency in the LTE/LTE-A systm.
- SPM used FLC as the core technique to calculate the supply voltage. Finding a better controller that can reduce more power is a challenging task.
- The used FLC in SPM has a rule table derived according to the observation of the power behaviour in digital circuits. Finding an optimization method to determine these rules will ensure a better reduction of power.
- Using log scaling as an input to the fuzzy logic solved the problem of high input range. Further investigation on this method is needed.
- Using SPM in the LTE systems can reduce a significant amount of power. The utilization of the clock frequency can reduce huge amount of power in LTE. LTE uses MIMO antenna to transmit the data. So there is another place in LTE where we can find another clock frequency diversity. This is another opportunity to reduce more power in the LTE system.

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APPENDIX A
PUBLISHED WORK

A.1. Published work.

During the period of study, the author published the following papers:

- "Power Reduction of a Mobile Device Processor Using FLC", Qusay Al-Doori and Dr. Omar Alani, The 15th annual postgraduate symposium on the coverage of telecommunication, networking and broadcasting. PGNET2014 in Liverpool 2014.
- "A Multi Polynomial CRC Circuit for LTE-Advanced Communication standard", Qusay Al-Doori and Dr. Omar Alani, proceedings of 7th Computer Science & Electronic Engineering Conference. Essex 2015.
- "An Intelligent Energy Manager Circuit for Long Term Evolution Communication System" Qusay Al-Doori and Dr. Omar Alani, IEEE transection on circuits and systems II: Express Briefs (under review).
- "Power approximation model in digital circuit design", Qusay Al-Doori and Dr. Omar Alani, IET, circuits, devices and systems. (under review).
- "A New Approach for Reducing Power in Digital Communication Systems Utilizing Dynamic Voltage / Frequency Scheduling", Qusay Al-Doori and Dr. Omar Alani, IET, circuits, devices and systems. (under review).